FOR MESSRS: DATE: April. 7. 2005

CUSTOMER'S SPECIFICATIONS
(Tentative Edition)

1,269cm (50 Inch) Wide Plasma Display Module

MODEL : **S50HW-YD01**

(PAL/NTSC)

* This specification will be approved by both DELL and Samsung SDI Co.,Ltd.
* Please return one of this specification with your signature for approval.

Proposed by: Approved by:

Signature **Signature** .

SAMSUNG SDI CO.,LTD.

Revision History

No	Date	Description Of Changes	Rev. no	Approval
1	April. 7. '05	Tentative Edition Initial Estabilished	Rev.0.0	
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1. Description

The S50HW-YD01 is a 50-inch wide full color plasma display Module with a resolution of 1366(H) × 768(V) pixels. The display module includes the Plasma Display Panel, the Panel Driving Electronics, the Logic Control Board, and the Power Supply Unit(PSU).

2. FEATURES

- Wide aspect ratio(16:9) 50 inch diagonal display screen. The display area is 1106.46mm wide and 622.08mm high.
- Slim and light weight. The display Module is 65.5mm in depth and weight only approx. 24.8kg include power supply.
- 68719.47 million colors(12Bit), 1073.7 million colors(10Bit), or 16.77 million colors(8Bit) combination of R,G and B digital data.(according to LVDS input selection)
- High Luminance, High contrast, Wide viewing angle. The screen has a white peak Luminance of typical 1,100 cd/? (TBD, NTSC)/1000 cd/? (TBD, PAL), contrast of typical 8,000:1(TBD, NTSC)/6000:1(TBD, PAL). And a viewing angle of greater than 160° comparable to those of CRTs.

3. PRODUCT NAME AND MODEL NUMBER

- Product name : 50 inch Full Color Plasma Display Module3 (abbreviation : PDP Module3)
- Model number : S50HW-YD01

4. FUNCTION OUTLINE

- The plasma display Module has an APC(Automatic Power Control) function which restricts power consumption within the certain value with regard to each display load ratio.
- The plasma display Module is operated by following digital video signals; Vertical synchronous signal, Horizontal synchronous signal, Enable signal and 8~12bits data signal of each R,G, and B color. All signals are based on LVDS level.
- The plasma display Module is operated at 50Hz or 60Hz frame rate. An external frame rate conversion is required in order to display the other formats.
- The plasma display Module requires several types of input power voltages ; voltage for LOGIC, voltage for TCP, voltage for Gate Driver, voltage for Sustain, Address, Set, Scan and X-bias.
- The plasma display Module is operated at progressive signal only. An external progressive scan conversion is required in order to display the other formats.
- The plasma display Module requires rated 100~240V, 50~60Hz of input power voltage.

5. BLOCK DIAGRAM

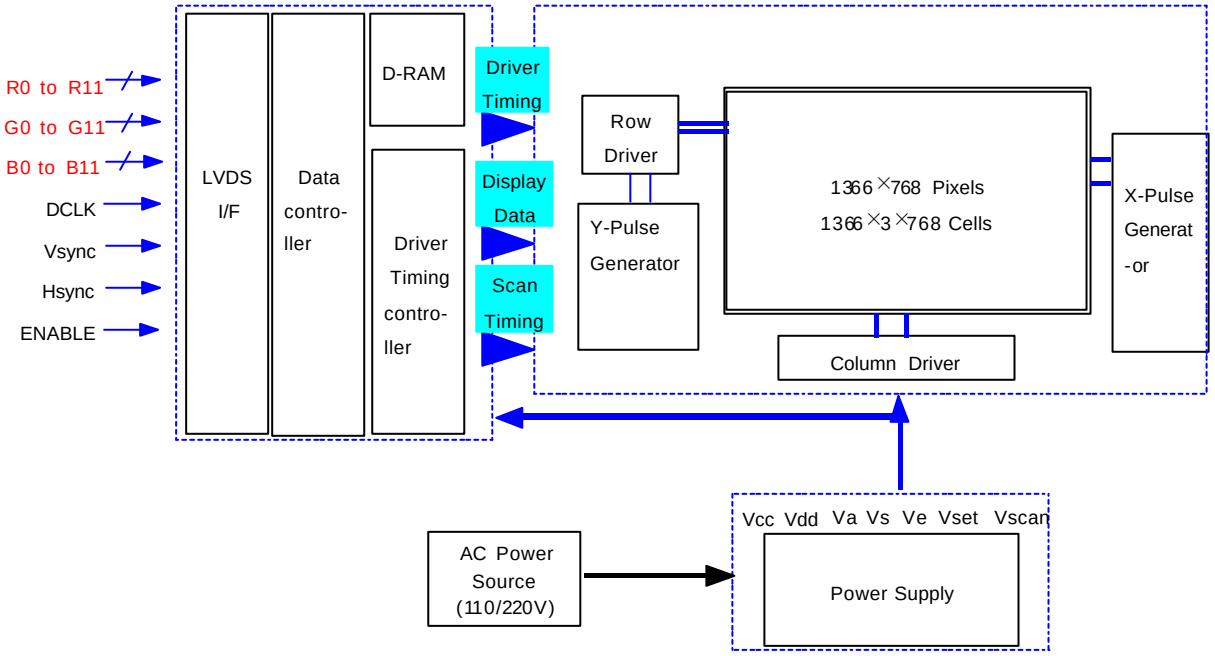

Figure-1. Block Diagram of PDP module

6. DISPLAY CHARACTERISTICS

6.1 Display Performance

No	Item	Rating	
1	Display Pixels	Horizontal 1366 × Vertical 768 pixels (1 pixel = 1 R,G,B cells)	
2	Display Cells	Horizontal 4,098 × Vertical 768 cells	
3	Pixel Pitch	Horizontal 810? × Vertical 810?	
4	Cell Size	R	Horizontal 270? × Vertical 810?
		G	Horizontal 270? × Vertical 810?
		B	Horizontal 270? × Vertical 810?
5	Pixel Type	R, G, B Stripe (refer to Figure-2)	
6	Effective Display Size	Horizontal 1106.46? × Vertical 622.08? [43.54 inch × 24.49 inch]	
7	Number of color	68719.47 million colors (12Bit) 1073.7 million colors (10Bit) 16.77 million colors (8Bit)	
8	Peak Luminance *1 (peak algorithm off)	NTSC : Typical 1,100 cd/? , Minimum 950 cd/? (Tentative) PAL : Typical 1,000 cd/? , Minimum 900 cd/? (Tentative)	
9	Peak Luminance *1 (peak algorithm on)	NTSC : Typical 1,300 cd/? , Minimum 1100 cd/? (Tentative) PAL : Typical 1,200 cd/? , Minimum 1000 cd/? (Tentative)	
10	Contrast Ratio *2 (in dark room, peak algorithm off)	NTSC : Typical 8,000:1, Minimum 5,000:1 (Tentative) PAL : Typical 6,000:1, Minimum 4,000:1 (Tentative)	
11	Contrast Ratio *2 (in dark room, peak algorithm on)	NTSC : Typical 10,000:1, Minimum 6,000:1 (Tentative) PAL : Typical 7,000:1, Minimum 5,000:1 (Tentative)	
12	Color Coordinates	Full White: x = 0.285± 0.015, y = 0.290± 0.015 (typical)	
13	Viewing Angle *3	Over 160°	

(Note)

* 1. Luminance and Color Coordinates are the values that were measured with 1% load ratio white pattern. The condition for measurement is shown in Figure-3.
* 2. Contrast Ratio is calculated from the display Luminance and the non-display Luminance value. Display condition is shown in Figure-4.
* 3. Viewing angle is a critical angle at which the Luminance is reduced to 50% to the Luminance perpendicular to the PDP Module. The Luminance is measured by a non-contact luminance meter BA-7.

6.2 Display Cell Arrangement

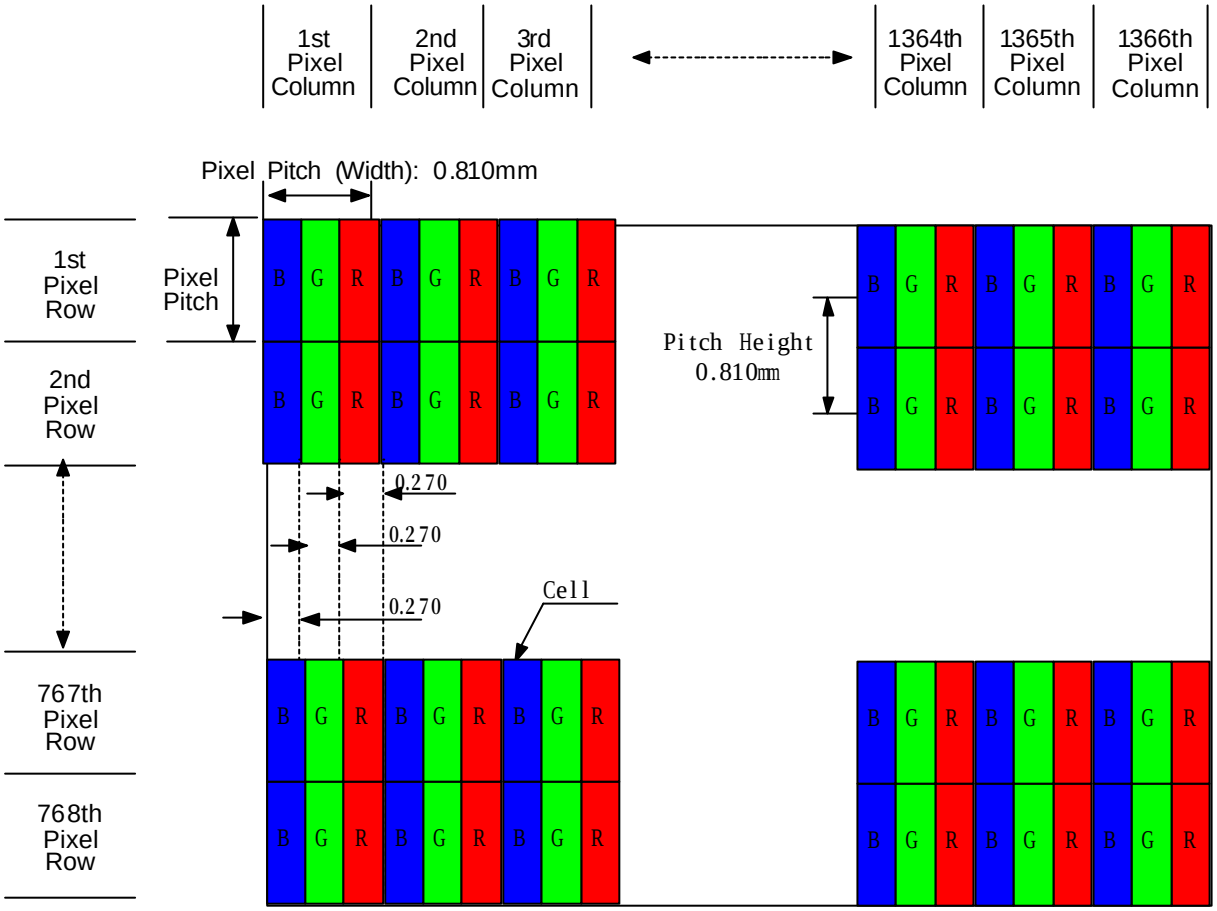

Figure-2. Display Cell Arrangement

6.3 Luminance Measurement Condition

(1) Display Pattern

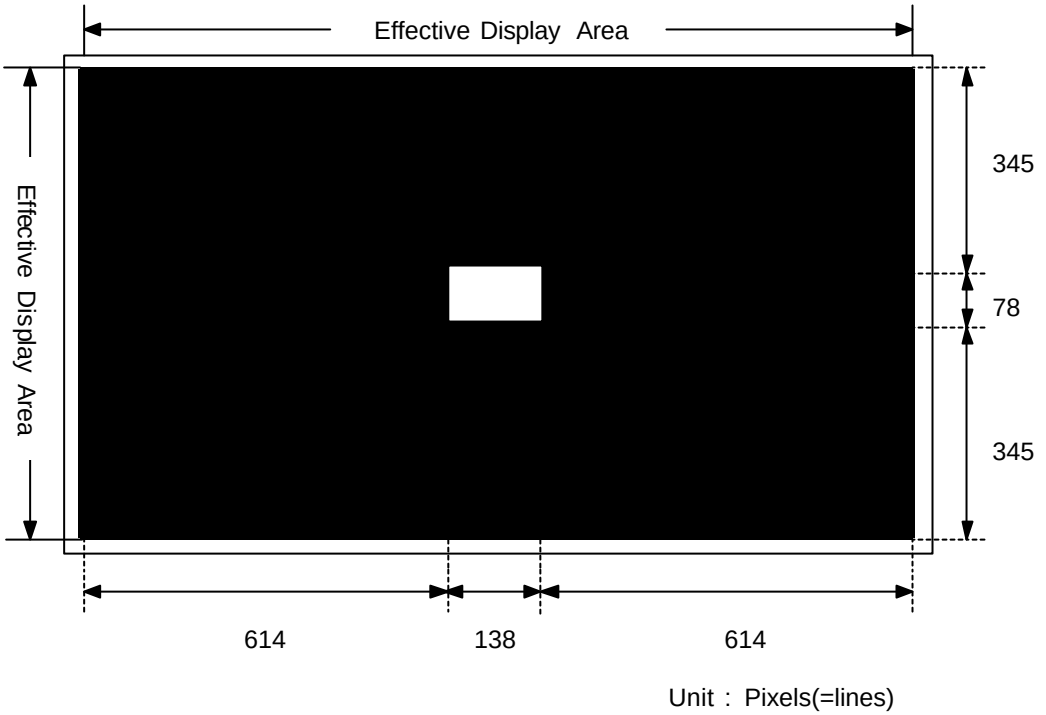

Figure-3. Display Pattern for Brightness & Contrast Ratio Measurement

(2) Display Area ratio : 1% white window

(3) Vsync : 16.7ms or 20ms

(4) Measuring equipment : MINOLTA CA-100Plus
Pattern Generator(VG-828, LVDS Output).

(5) Ambient Temperature : Room Temperature

(6) Ambient Luminance : Dark Room (<2 lux)

[Note]

1. Measurement is done within 5 seconds after Power On. The temperature of panel before measurement is room temperature (25?).

6.4 Contrast Measurement Condition

(1) Measuring point

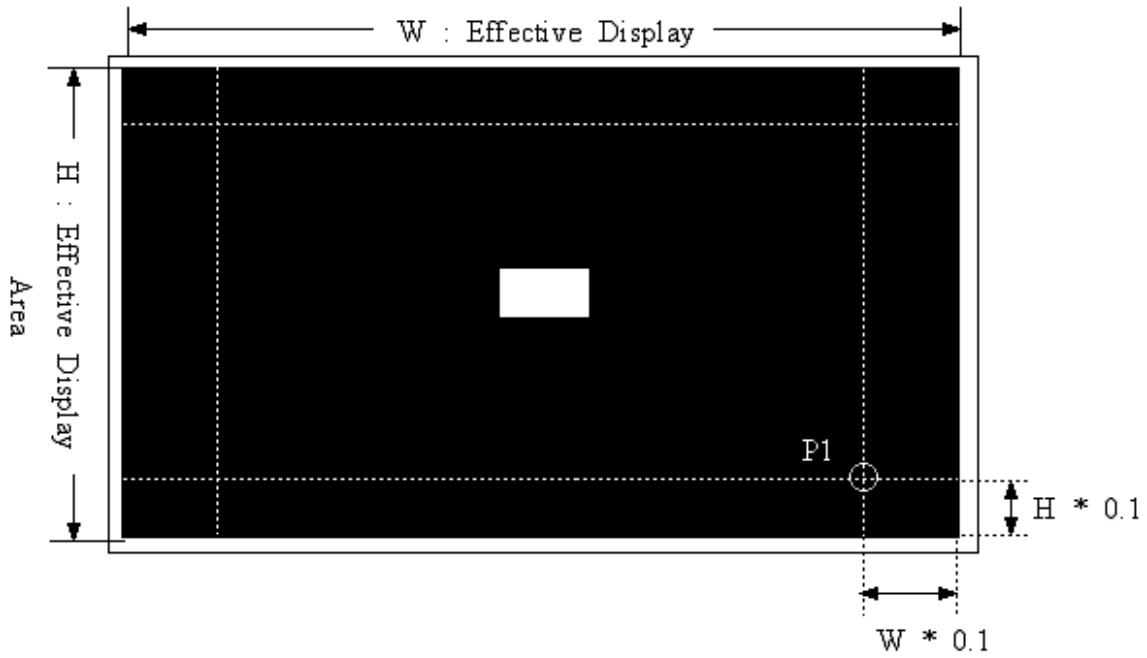

Figure-4. Measurement point

(2) Vsync : 16.7 ms or 20ms

(3) Measuring Equipment : MINOLTA CA-100Plus
Pattern Generator(VG-828, LVDS Output).

(4) Contrast Calculation formula

$$\text{Contrast ratio} = \frac{\text{Luminance of 1\% white window Area at the center of the screen}}{\text{Luminance of Black Area *1}}$$

? Note ?

1. For mass production test purposes, it is recommended to measure just 1 point, P1 of Figure.-4 on display pattern of Fig.-3.

(5) Ambient Light : Dark Room (<2 lux)

6.5 Display Cell Defect Specification

In some cases, a panel may have defective cells that cannot be controlled.
These defective cells can be categorized into three types;
(1) Non-lighting cell defect : defect in which the cell is always off
(2) Non-extinguishing cell defect : defect in which the cell is always on
(3) Flickering cell defect : defect in which the cell is flickering.
(4) High intensity cell defect : defect in which the cell is brighter than other cells
(5) Test Pattern : Full White, Full Red, Full Green and Full Blue with 1023 gray level.

The display cell defect specifications define the allowed limits for display cell defects and are used as the criteria in determining whether a panel should be shipped.

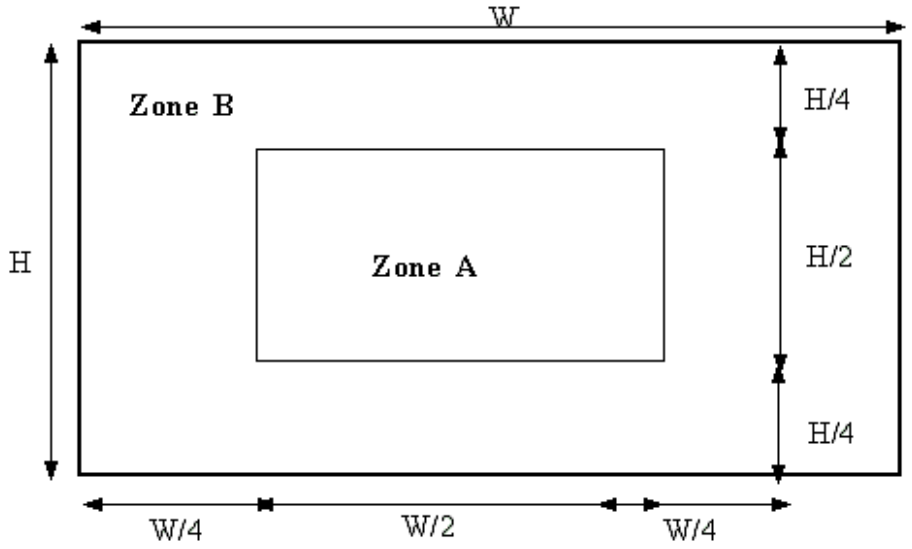

Figure-5. Measurement Area

Item	Specification	
	Number of cell defects	
Non-lighting cell defect	**Zone A: 4 and less**	**Zone B: 10 and less**
Non-extinguishing cell defect	**Zone A: zero**	**Zone B: zero**
Flickering cell defect	**Zone A: zero**	**Zone B: zero**
Continuous cell defect	**Zone A: zero**	**Zone B: zero**
Total defect	**Total number of cell defects in Zone A and B is less than 12**	

6.6 Brightness Variation Specification

The color-PDP uses ultraviolet light produced by gas discharge to illuminate phosphor. Uneven phosphor coating and inconsistent discharge characteristics cause slight difference in brightness among the sections in a panel.

Item	Definition	Specification
Full white brightness variation	The brightness is measured at 9 points (A1~A9 of Fig-6) on full white pattern. The full white brightness variation as then calculated from the following equations.	10% and less
Equation	$\frac{Max - \bar{x}}{\bar{x}} \times 100\%$ & $\frac{\bar{x} - Min}{\bar{x}} \times 100\%$	

The brightness variation specifications define the allowed limits for brightness differences and the criteria in determining whether a panel is shipped.

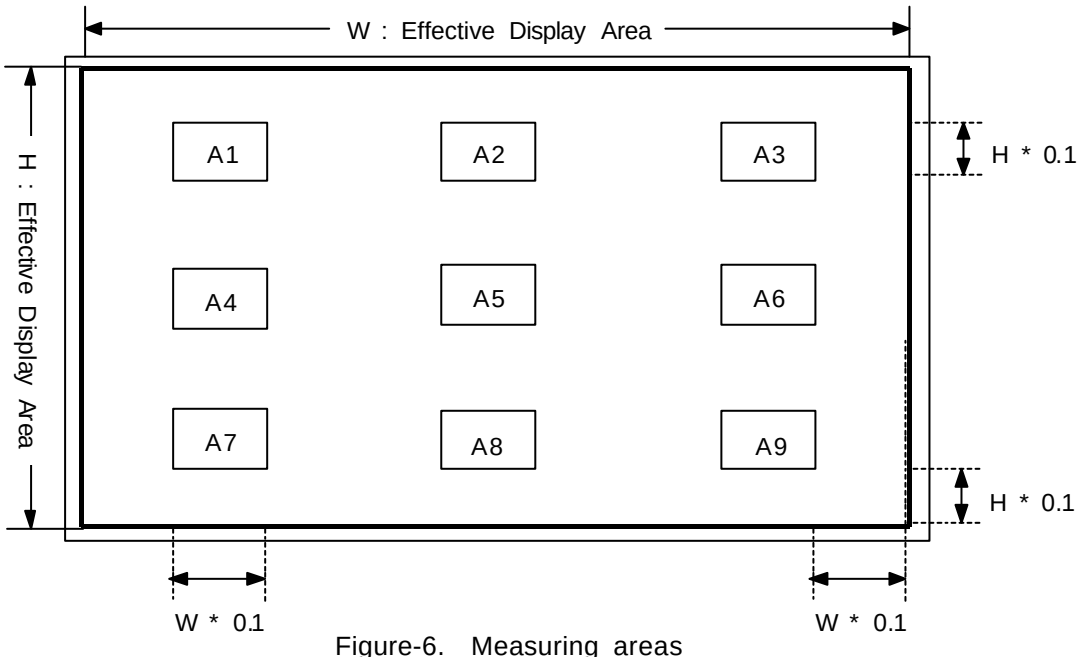

Figure-6. Measuring areas

6.7 Power consumption

6.7.1 APC (Automatic Power Control) Function

The PDP has an APC (Automatic Power Control) function for the panel driver power source. When the total display load ratio exceeds approximately 10%, total power consumption is limited within a specified level(=Lower Power Limit) by APC function.
The operation behaviour of APC function is called as SLOW-APC. When the display load-ratio changes from low to high value, the power-consumption rises instantly to "Upper Power Limit" and gradually decreases until it reachs to the "Lower Power Limit".

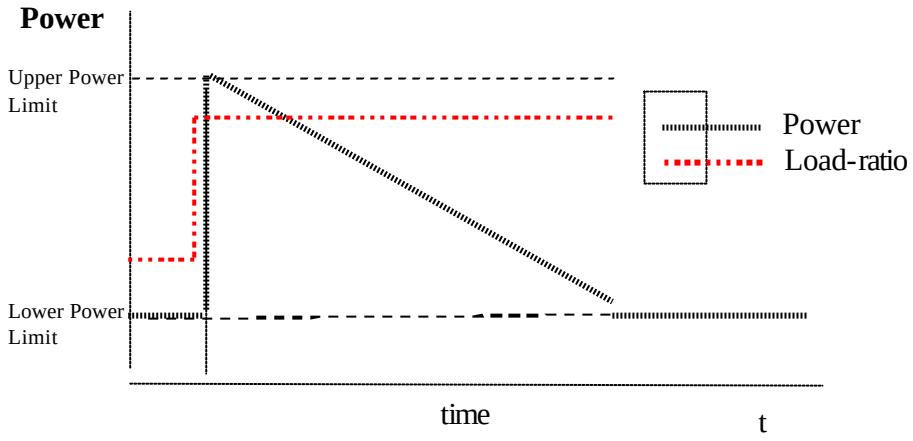

Figure-7 Slow APC Behaviour

6.7.2 Brightness and Power Mode Control

This PDP module offsers two methods for Brightness and Power mode control.
One is APCO(APC Offset) for Peak-Brightness control, and the others are PUG and PLG for power mode control. APCO, PUG and PLG are registers controllable through I2C communication from image B'd. For a detailed address and data bits of these registers , refer to the Chapter 11. Address Map.

(1) Peak-Brightness Control(APCO)
- controls the max.sustain number
- APCO variable range : 00~C7h

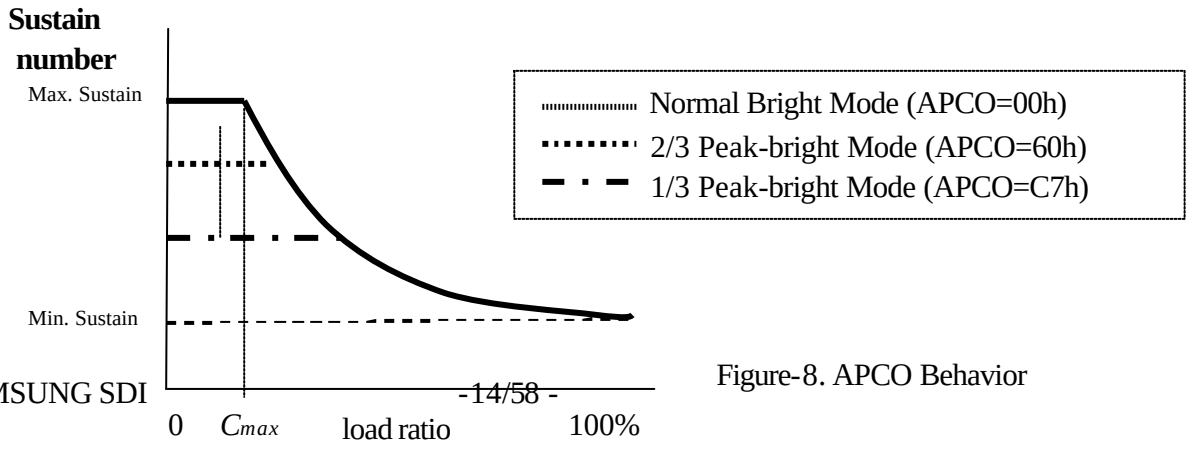

Figure-8. APCO Behavior

(2) Power-Mode Control (**PUG, PLG**)

- PUG(Power Upper Gain control register)
- PLG(Power Lower Gain control register)
- Variable range : 00 ~ FFh(Tentative) , Default Value : 80

PUG is for controlling upper power level and PLG is for lower power level.
PUG(PLG) value larger than the default makes more power consumption, and smaller value makes less power.

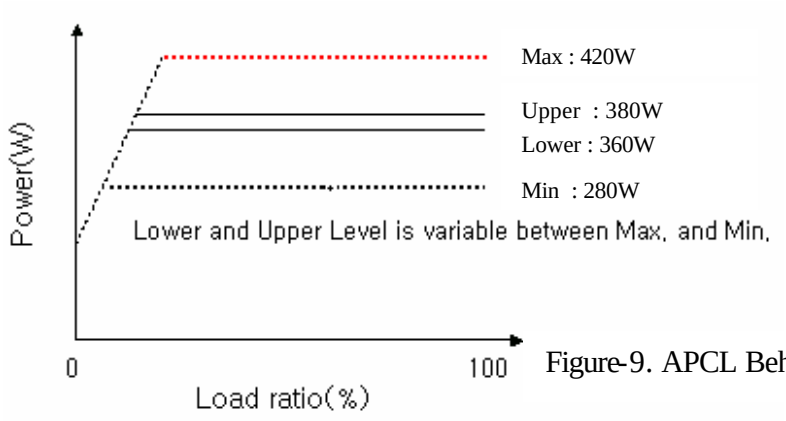

Figure-9. APCL Behavior

6.7.3 Power Consumption Specification

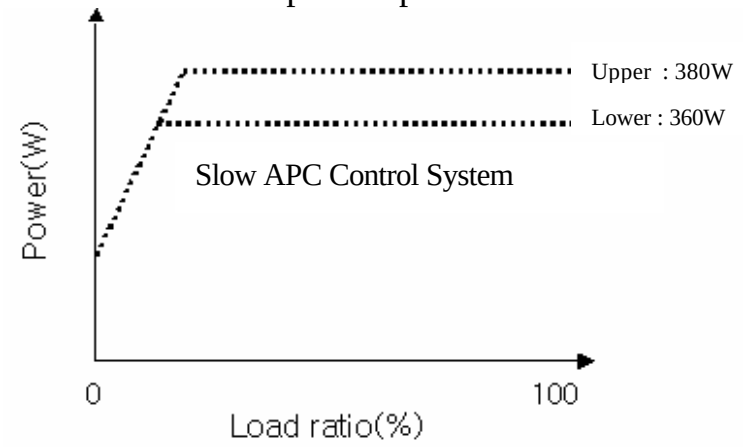

Figure-10. Display load ratio vs. Power consumption

Mode	Maximum Level	Typical Level	Minimum Level	Remarks
Standard PUG=80h PLG=80h	420W (Tentative)	380W 360W (Tentative)	280W (Tentative)	Typical level can be controled by customer. Maximum level and Minimum level are not fixed.

[Note]

1.This is the case that the PDP Module includes SDI's Main PSU at AC 100V, 60Hz.
It is measured on full screen white pattern with input gray-level 1024(10Bit) in module.

3. Power consumption is same for PAL and NTSC mode.

6.8 Gamma characteristics

This PDP module offsers Customer's Gamma selection and Gamma control.
Registers are controllable through I2C communication from image B'd. For a detailed address and data bits of these registers , refer to the Chapter 11. Address Map.

6.8.1 Basis of Gamma Curve

This PDP module is normally applied to the 2.2 gamma curve (refer to Figure-11)
But this specification could be modified on the request of the customer

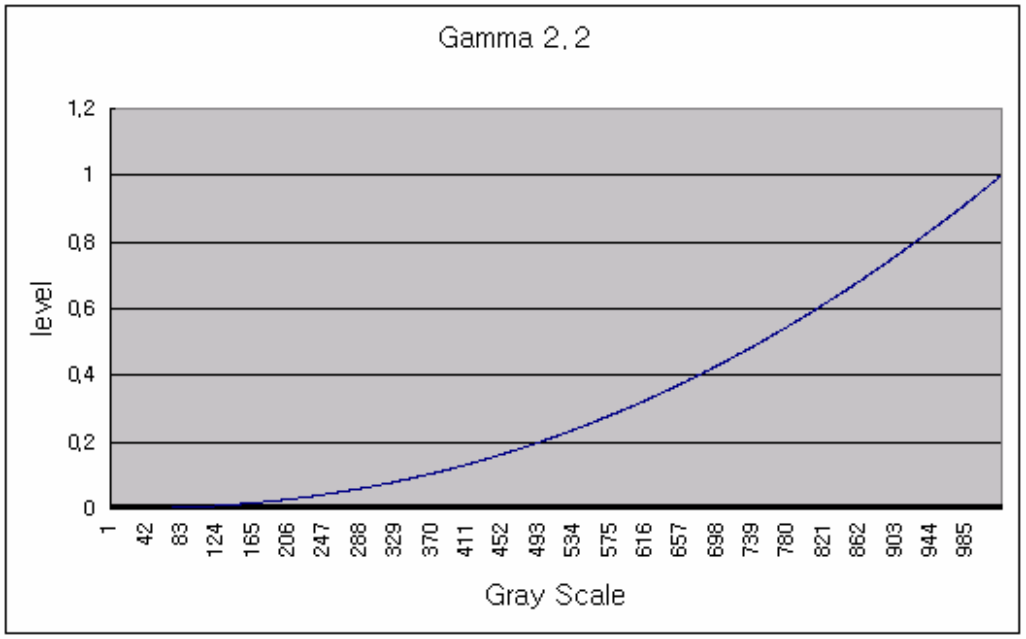

Figure-11. Default Gamma Curve

6.8.2 Multi Gamma Table

The PDP module can have 5 different Gamma curve that can be selected by customer.
4 pre-determined curves are stored in logic board. They are No.0 (r = 2.0), No.1(r = 2.1), No.2(r = 2.2), No.3(r = s curve). No.4 Gamma curve can be editable by Set Maker.
Set Maker can reshape the default gamma by gain control factor.

6.8.3 Control of Gamma Table

GTSEL(Gamma Table Selection) is for the change gamma table. GTSEL is the register controllable through I2C communication from image B'd. For a detailed address and data bits of this register, refer to the Chapter 11. Address Map.

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7. SOUND PRESSURE LEVEL SPECIFICATION

7.1 Measurement Condition

(1) Background Noise Level : less than 20dBA
(2) Measuring Pattern : Dynamic Images (only, Full Black to Full White)
(3) Measuring Equipment : Sound level meter Type 2827 made by B&K
(4) Measuring Distance : 1m from the rear side of PDP Module
(5) Measuring point

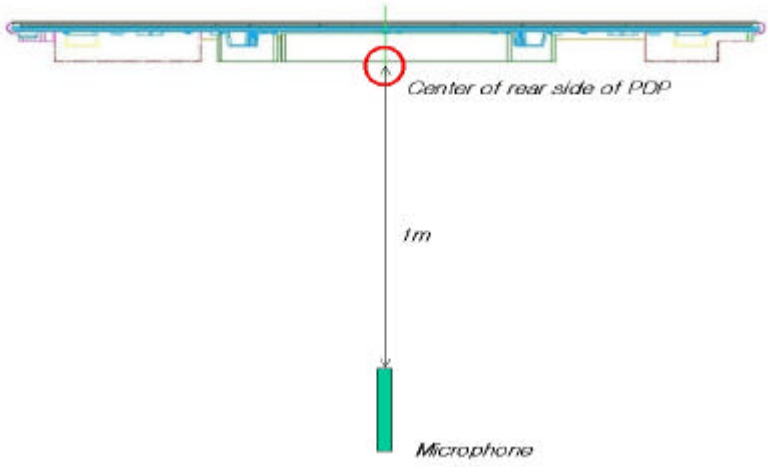


Figure-12. Measuring Point

7.2 Sound Pressure Level :

(1) Overall level
- Sound Pressure Level caculated from the individual band levels of 50Hz ~ 8kHz.
- Specification : 30dB max.

(2) High Frequency level
- Sound Pressure Levels of individual band levels between 1kHz ~ 8kHz.
- Specification : 14dB max.

8. MECHANICAL CHARACTERISTICS

8.1 Mechanical Specifications

No	Item	Rating
1	Outer Dimension	Width 1,175 mm × Height 682 mm × Thickness 65.5 mm (include FPC and TCP) *see Appendix : Mechanical Dimension Drawing
2	Weight	Approximatly 24.8 kg

8.2 Mechanical Characteristics

No	Item	Rating
1	Vibration	Frequency : 10 ~ 55 Hz Sweep Rate : 1 Octave/min Stroke : x,y direction : 0.35 mm Z direction : 0.175 mm
2	Shock	Acceleration : less than 20 G (x,y direction) less than 10 G (z direction) Duration Time : 11 ms

***** Notes: (Test condition) Non-Packaging, Operational (only for Vibration)
* Test time of Vibration Test is 30 minutes every direction(x,y,z)
* The number of times for shock test is 6 times every direction(x,y,z).

9. ENVIRONMENTAL CONDITIONS

9.1 Operational Environmental Condition

No	Item	Rating	
1	Ambient Temperature	Fuctional Operation *1	-10? ~ 70?
		Display Operation *2	0? ~ 50?
		Temperature Slope	Below 1.5 ? /minute
2	Panel Surface Temperature *3	Small Size Pattern Full White Pattern	~ 110 ? ~ 75 ?
		Temperature Slope	Below 20 ? /cm
3	Humidity	Fuctional Operation *1	5 ~ 90 RH (no condensation)
		Display Operation *2	20 ~ 80 RH (no condensation)
4	Pressure	Fuctional Operation *1	1,013 ~ 795 hPa (0 ~ 3,000 m)
		Display Operation *2	1,013 ~ 845 hPa (0 ~ 2,000 m)

[NOTE]

1. Functional Operation means that the PDP module is operated only its electrical function.
2. Display Operation means that the PDP module is operated in its full specifications.
3. Panel Surface Temperature means the surface temperature of panel that is just increased due to the loss of power inside Panel during the image display at a normal display mode and a ambient temprature defined in this table.
   The judgement of display defects (e.g. weak discharge, missing discharge) should be done when the panel is operated at a ambient temperature defined in this table.

9.2 Storage Environmental Condition *1

No	Item	Rating
1	Ambient Temperature	-20? ~ 70?
2	Humidity	5 ~ 85 RH (no condensation)
3	Pressure	300 ~ 1,013 hPa (0~10,000m)

[NOTE]

1. Storage means the short term period. (e.g. transportation, relocation and so on)

9.3 Panel Surface Condition

9.3.1. Panel surface temperature specification

The panel surface temperature should be kept as below in order to get stable display of image.

- Tp= below 110? (Absolute Maximum Rating); when small size of image is displayed
- Tp= below 75? ; when Full White is displayed.

If the temperature exceeds above level, it may cause the defects of display image like dot missing, line missing and/or poor image.

As the surface temperature of panel has tendency to rise with deduction of display rate, the relation with temperature can be describe as below:

75? (display load rate is high : Large Area)

~ 110? (display load rate is low : Small Area)

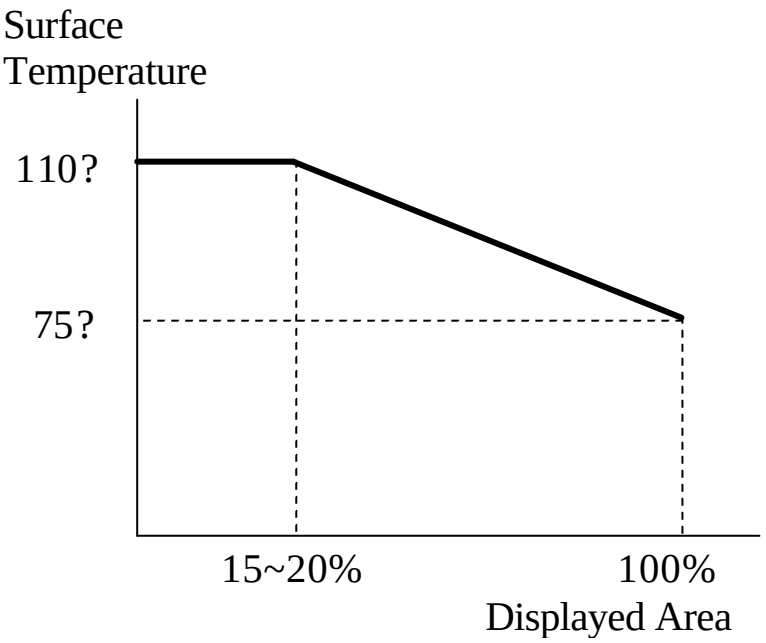


Figure-13. Surface Temperature Vs Displayed Area

It is strongly recommended that the panel surface temperature should be kept as low as possible, eventhought its maximium rating is descreibed as above.

9.3.2. Panel Surface Temperature for Breaking

The temperature uniformity across panel should be maintained below 20? /? not to occure panel breaking by temperature difference.

This breaking temperature is not absolute temperature, because it depends on condition of panel production and panel scratch. Please take this value as a reference.

10. Interface Signal Specifications

10. 1 Configuration Context

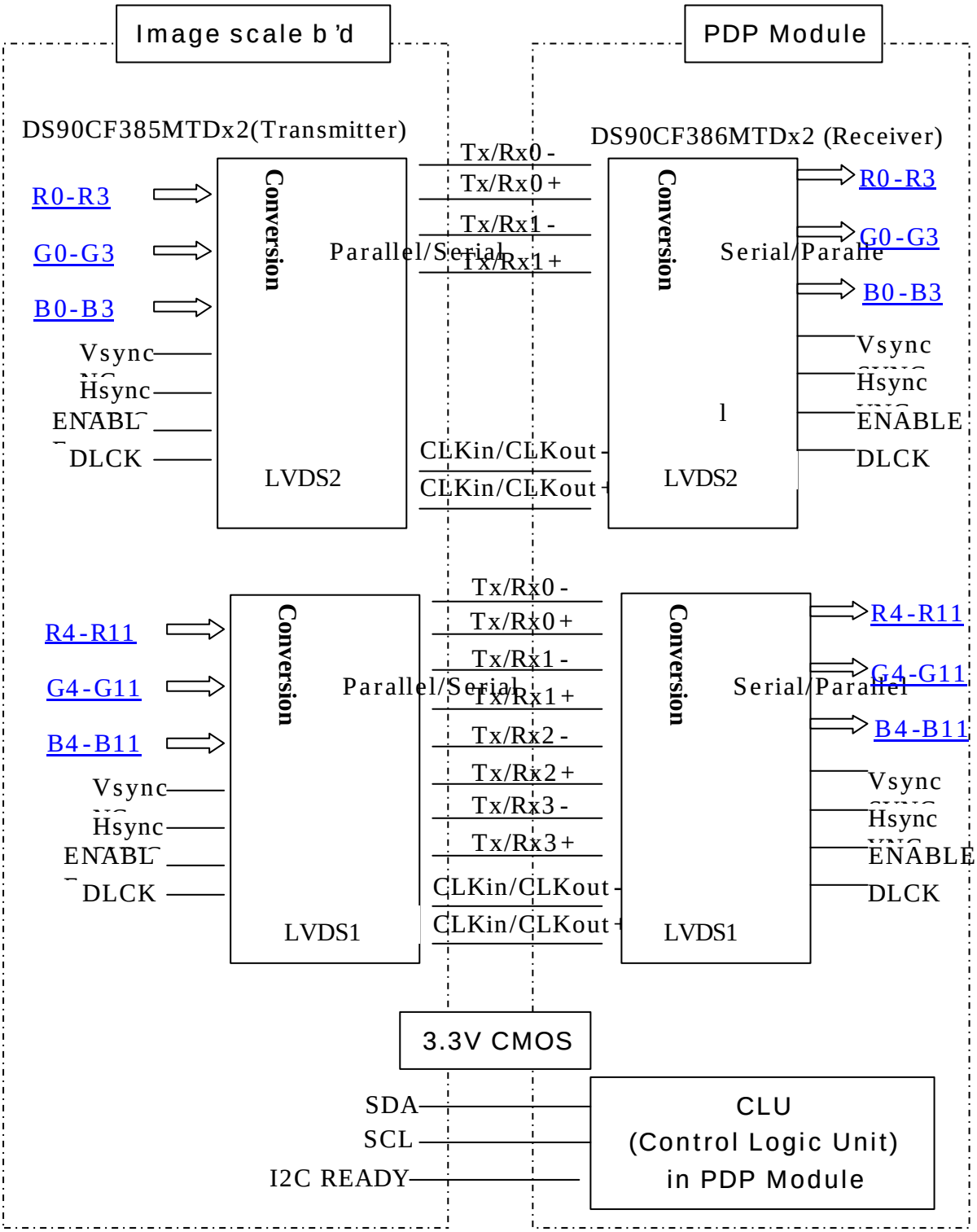


Figure- 14. Interface Signal (8~12bit)

10. 2. Interface Function Specifications (input data and display processing)

- 1366-dot data signals are inputted to this product to display data.
- The Video signal and control signal input section uses a low voltage differential signaling (LVDS) interface.
- An I2C bus serial data interface is used for the communication between MPU of FTV side and the CLU (Control LOGIC Module) of this PDP Module.
- I2C_READY signal is used that the CLU(Control LOGIC Unit) of PDP module inform image scale b'd that CLU is ready for I2C communication.(1 : ready, 0 : not ready)

10. 3. Input Signal Definition

No	Item	Signal name		Q	I/O	Method	Definition
1	Display Signal	Video Signal	RXIN0- RXIN0+ RXIN1- RXIN1+ RXIN2- RXIN2+ RXIN3- RXIN3+	1 1 1 1 1 1 1 1	Input (LVDS1)	LVDS Differentials	Differential serial data signal. Input video and timing signals after differential serial conversation using a dedicated transceiver. The serial data signal is transmitted seven times faster than the base signal.
			RXIN0- RXIN0+ RXIN1- RXIN1+	1 1 1 1	Input (LVDS2)		
		Dot Clock	RXCLKIN- RXCLKIN+	1 1	Input (LVDS1)	LVDS Differential	Differential clock signal. Input the clock signal after differential conversation using a dedicated transceiver. The clock signal is transmitted at the same speed as the base signal.
			RXCLKIN- RXCLKIN+	1 1	Input (LVDS2)		
2	MPU Communication	Communication	SDA SCL I2C_READY	1 1 1	Input	LVTTL (I2C)	I2C bus serial data communication signal. Communication with the CLU (Control Logic Module) of this product is enabled.

10. 4. LVDS Signal Definition and Function

A video signal (display data signal and control signal) is converted from parallel data to serial data with the LVDS transmitter and further converted into four sets of differential signals before inputted to this PDP Module. These signals are transmitted seven times faster than the dot clock signals. The dot clock signal is converted into one set of differential signals.
The LVDS signal definitions and functions are as follows (in Italic)::

[8~12 Bit LVDS Interface]

Interface Signal Function				
Symbol		I/O	Function	Remarks
LVDS1	*RxIN0-*	I	Display Data Signal:	LVDS signal
	RxIN0+	I	R4~R9,G4	LVDS signal
	RxIN1-	I	Display Data Signal:	LVDS signal
	RxIN1+	I	G5~G9,B4,B5	LVDS signal
	RxIN2-	I	Display Data Signal:	LVDS signal
	RxIN2+	I	B6~B9,HSYNC,VSYNC,DEN	LVDS signal
	RxIN3-	I	Display Data Signal:	LVDS signal
	RxIN3+	I	R10,R11,G10,G11,B10,B11	LVDS signal
	RxCLKin-	I	Dot Clock Signal:	LVDS signal
	RxCLKin+	I	Dot Clock	LVDS signal
LVDS2	RxIN0-	I	Display Data Signal:	LVDS signal
	RxIN0+	I	R2,R3,G2,G3,B2,B3	LVDS signal
	RxIN1-	I	Display Data Signal:	LVDS signal
	RxIN1+	I	R0,R1,G0,G1,B0,B1	LVDS signal
	RxIN2-	I	Display Data Signal:	LVDS signal
	RxIN2+	I	(GND)	LVDS signal
	RxCLKin-	I	Dot Clock Signal:	LVDS signal
	RxCLKin+	I	Dot Clock	LVDS signal
SDA		I	I2C serial data	3.3V CMOS
SCL		I	Clock signal for SDA	3.3V CMOS
I2C_READY		O	I2C enable signal	3.3V CMOS

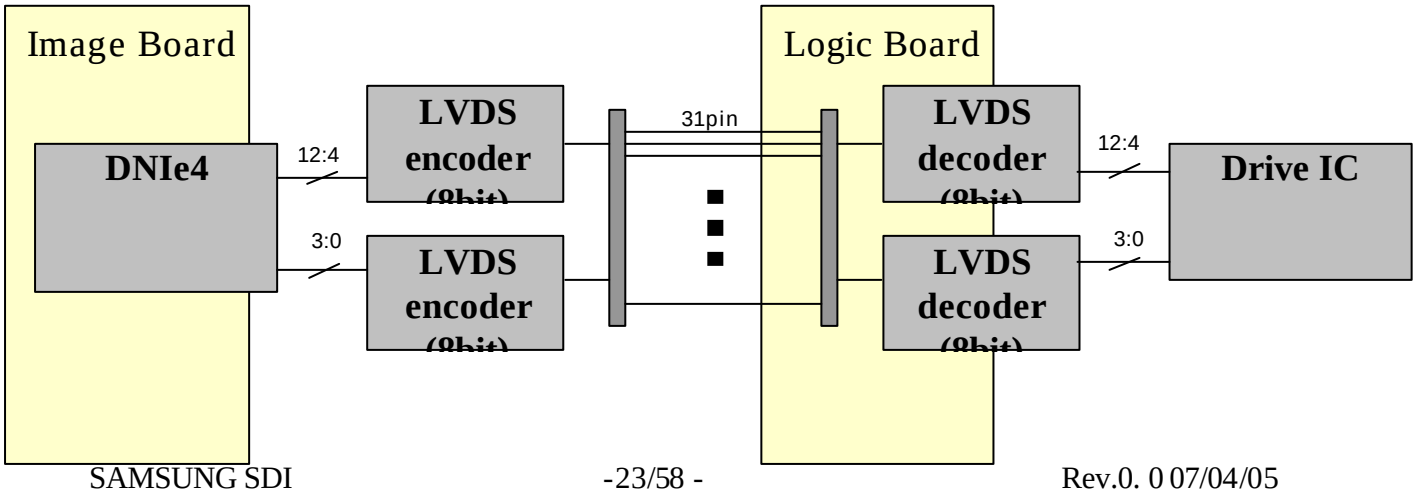


Figure- 15 LVDS 12bit application

10.5 LVDS Signal Pin Assignment

The table below indicates pin assignment of the LVDS IC(Transmitter & Receiver).
In the 12bit input mode, for other input bit mode, refer to technical references

Tx SIGNAL(Image Board) (DS90C385x2, National)							
	PIN No	PIN NAME	SIGNAL		PIN No	PIN NAME	SIGNAL
LVDS1	31	TxCLKIN	Dot Clock	LVDS2	31	TxCLKIN	Dot Clock
	51	TxIN0	R(4)		51	TxIN0	R(2)
	52	TxIN1	R(5)		52	TxIN1	R(3)
	54	TxIN2	R(6)		54	TxIN2	G(2)
	55	TxIN3	R(7)		55	TxIN3	G(3)
	56	TxIN4	R(8)		56	TxIN4	B(2)
	2	TxIN5	R(11)		2	TxIN5	N.C.
	3	TxIN6	R(9)		3	TxIN6	B(3)
	4	TxIN7	G(4)		4	TxIN7	N.C.
	6	TxIN8	G(5)		6	TxIN8	R(0)
	7	TxIN9	G(6)		7	TxIN9	R(1)
	8	TxIN10	G(10)		8	TxIN10	N.C.
	10	TxIN11	G(11)		10	TxIN11	N.C.
	11	TxIN12	G(7)		11	TxIN12	G(0)
	12	TxIN13	G(8)		12	TxIN13	G(1)
	14	TxIN14	G(9)		14	TxIN14	B(0)
	15	TxIN15	B(4)		15	TxIN15	B(1)
	16	TxIN16	B(10)		16	TxIN16	N.C.
	18	TxIN17	B(11)		18	TxIN17	N.C.
	19	TxIN18	B(5)		19	TxIN18	N.C.
	20	TxIN19	B(6)		20	TxIN19	HSYNC
	22	TxIN20	B(7)		22	TxIN20	VSYNC
	23	TxIN21	B(8)		23	TxIN21	DEN
	24	TxIN22	B(9)		24	TxIN22	N.C.
	25	TxIN23	N.C.		25	TxIN23	N.C.
	27	TxIN24	HSYNC		27	TxIN24	N.C.
	28	TxIN25	VSYNC		28	TxIN25	N.C.
	30	TxIN26	DEN		30	TxIN26	N.C.
	50	TxIN27	R(10)		50	TxIN27	N.C.

[**Pin assignment Of Transmitter**]

Rx SIGNAL(Logic Board) (DS90CF386x2 ,National)							
	PIN No	**PIN NAME**	**SIGNAL**		**PIN No**	**PIN NAME**	**SIGNAL**
LVDS1	26	RxCLKOUT	Dot Clock	LVDS2	26	RxCLKOUT	Dot Clock
	27	RxOUT0	R(4)		27	RxOUT0	R(2)
	29	RxOUT1	R(5)		29	RxOUT1	R(3)
	30	RxOUT2	R(6)		30	RxOUT2	G(2)
	32	RxOUT3	R(7)		32	RxOUT3	G(3)
	33	RxOUT4	R(8)		33	RxOUT4	B(2)
	34	RxOUT5	R(11)		34	RxOUT5	N.C.
	35	RxOUT6	R(9)		35	RxOUT6	B(3)
	37	RxOUT7	G(4)		37	RxOUT7	N.C.
	38	RxOUT8	G(5)		38	RxOUT8	R(0)
	39	RxOUT9	G(6)		39	RxOUT9	R(1)
	41	RxOUT10	G(10)		41	RxOUT10	N.C.
	42	RxOUT11	G(11)		42	RxOUT11	N.C.
	43	RxOUT12	G(7)		43	RxOUT12	G(0)
	45	RxOUT13	G(8)		45	RxOUT13	G(1)
	46	RxOUT14	G(9)		46	RxOUT14	B(0)
	47	RxOUT15	B(4)		47	RxOUT15	B(1)
	49	RxOUT16	B(10)		49	RxOUT16	N.C.
	50	RxOUT17	B(11)		50	RxOUT17	N.C.
	51	RxOUT18	B(5)		51	RxOUT18	N.C.
	53	RxOUT19	B(6)		53	RxOUT19	HSYNC
	54	RxOUT20	B(7)		54	RxOUT20	VSYNC
	55	RxOUT21	B(8)		55	RxOUT21	DEN
	1	RxOUT22	B(9)		1	RxOUT22	N.C.
	2	RxOUT23	N.C.		2	RxOUT23	N.C.
	3	RxOUT24	HSYNC		3	RxOUT24	N.C.
	5	RxOUT25	VSYNC		5	RxOUT25	N.C.
	6	RxOUT26	DEN		6	RxOUT26	N.C.
	7	RxOUT27	R(10)		7	RxOUT27	N.C.

[**Pin assignment Of Receiver**]

10. 6 Video Signal Definition and Function

The table below indicates the definitions and functions of input video signals before LVDS conversion.

Interfaces Signal Functions		
Symbol	**Function**	**Remarks**
R11(7) to R0	12(8) bits red video signal (note 1)	Display data signal: R12(8): MSB*, R0: LSB**
G11(7) to G0	12(8) bits green video signal (note 1)	Display data signal: G12(8): MSB*, G0: LSB**
B11(7) to B0	12(8) bits blue video signal (note 1)	Display data signal: B12(8): MSB*, B0: LSB**
Hsync	Horizontal synchronous signal	This signal specifies the data period for one horizontal line. Control of the next line begins at the rising edge of Hsync.
Vsync	Vertical synchronous signal	Timing signal that controls the start of the screen. Control of the next screen begins at the rising edge of Vsync.
DCLK	Clock for video signal	Latch the video signal at falling edge.

* MSB: Most Significant Bit
**LSB: Least Significant Bit

Note 1: The RGB signal may be compensated with Inverse γ circuit (E/D (=Error Diffusion) must be included) before inputted to the PDP Module. In order to obtain good characteristic of low level's gray scale, inverse γ correction and E/D process are advisory to be performed after inputted to the PDP Module.

Note 2 : Reommended Transmitter ? DS90CF385x2

10.7 Electrical Condition of Interface Signal

10.7. 1. Maximum Ratings

Common conditions : Ta = 25? , Vcc = 3.3V

Absolute Ratings						
Item			**Parameter**	**Symbol**	**Ratings**	**Module**
Input Signals	LVDS	Rx0-/+,Rx1-/+,Rx2-/+, Rx3-/+, Rx4/+, CLKin-/+	**Input Voltage**	**Vi**	**-0.3~ 3.6**	**V**
			Input Current	**Ii**	**-10~10**	**?**
	3.3V CMOS	SDA, SCL	Input Voltage	Vi	**-0.5~3.6**	V
			Input Current	**Ii**	**-15**	**?**

10.7. 2. Electrical Characteristics

Common conditions : Ta = 0? ~ +70? , Vcc = 3.0V ~ 3.6V

Electrical Characteristics							
Signal	**Item**	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Module**
LVDS	High level input voltage	V_{th}	V_{CM}=1.2V	-	-	100	?
	Low level input voltage	V_{tl}	V_{CM}=1.2V	-100	-	-	?
	Input current	I_{in}	V_{IN} = +2.4V/0V Vcc = 3.6V	-	-	± 20.0	?
I2C	Input Voltage	V_{ih}		0.5*Vcc	-	4.1	V
		V_{il}		-0.5	-	0.3*Vcc	V
	Input Capacitance	V_{in}	-	-	-	8	?
	Output Voltage	V_{oh}	I_{oh} = 8 ?	2.4	-	-	V
		V_{ol}	-	-	-	0.4	V
	Output Current	I_{ol}	-	-	-	10	?
3.3V CMOS	High level input voltage	V_{ih}	-	2.0	-	-	V
	Low level input voltage	V_{il}	-	GND	-	0.8	V
	Input current	I_i	V_I=Vcc or GND	-	-	± 10.0	?
	High level output voltage	V_{oh}	Io = -1 ?	2.4	-	-	V
	Low level output current	V_{ol}	I_o = 1 ?	-	-	0.4	V

10. 8 Video Signal Interface Timing Conditions

The table below indicates the conditions of input video signal before LVDS conversion. These conditions must be satisfied. Refer to the figure of the timing chart.

8 bits LVDS ~12 bit LVDS belong to one timing table below.

Video Input Signal Timing (NTSC/PAL)			
Symbol	**Timing**	**Unit**	**Remarks**
T_{VSYNC}	Refer to 'Remark'	?	- PAL long mode : below 48Hz - PAL Normal Mode : 48 ~ 52Hz - PAL LB Mode : 52 ~ 55 Hz - NTSC long Mode : 55 ~ 58 Hz - NTSC Normal Mode : 58 ~ 62 Hz - NTSC LB Mode : 62 ~ 65 Hz - NTSC Mask Mode : above 65 Hz * LB Mode(=Low Brightness Mode) : By decreasing sustain period on the Tvsync shorter than normal, brightness is reduced. * Mask(or Flicker) Mode : Masks abnormally short Vsync, and displays at the frame period twice as input Vsync period. * long mode : mode change is not occurred in this peried, the display is normally operation by increasing the Vsync period.
T_{VHS} **(1frame)**	810(Min.)	Hsync	No. of Hsync in 1 Vsync Period
T_{WV}	2(Min.)	Hsync	Vsync on time
T_{VH}	8(Min.)	Hsync	Vsync back porch
T_{HV}	34(Min.)	Hsync	Vsync front porch
T_{HSYNC}	19.6(Min.)	?	Hsync width
T_{WH}	6(Min.)	Dclk	Hsync on time
T_{HC}	750(Min.)	?	Hsync back porch
T_{CH}	380(Min)	ns	Hsync front porch
T_{CLK}	71 ~ Tclk_Max	MHz	Dot clock(DCLK) frequency Tclk_max = (1366*74)/(1366+(750- T_{HC})*74*0.001) Ex) if T_{HC} = 800ns, Tclk_max = 74.2MHz
T_{SUD}	5	?	Minimum Data setup time
T_{HD}	5	?	Minimum Data hold time

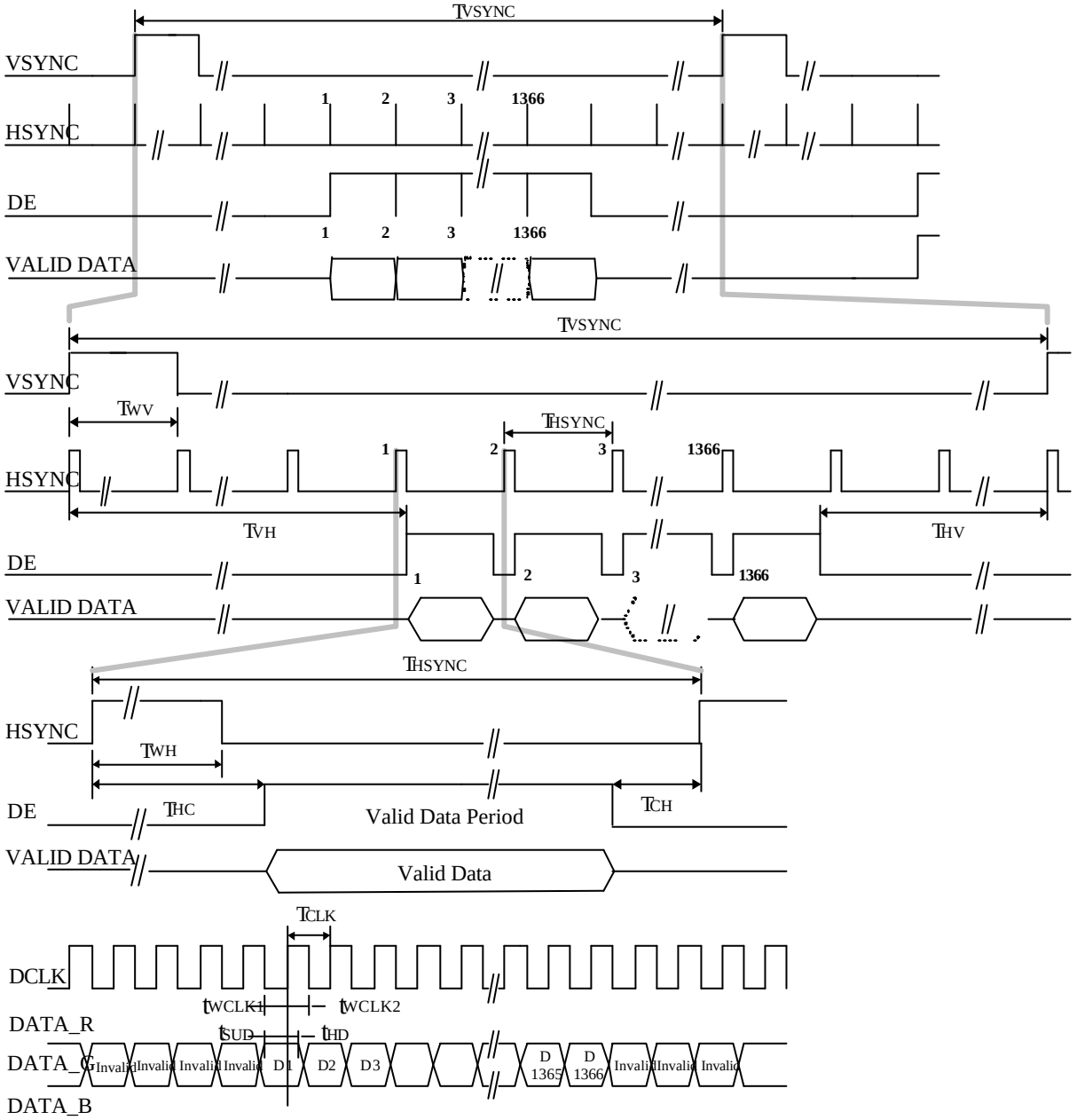


Figure-16. Video Input Signal Timing Chart

10. 9 LVDS Interface Timing Conditions

This PDP Module uses an LVDS interface for the signal input. For details of the input signal timing conditions, refer to the data sheets prepared by the LVDS transmitter IC maker. This PDP Module uses **National Semiconductor (www.national.com)**'s DS90CF386

10. 10 LVDS Connection Specifications

The following Figure shows the connection specifications and signal assignments of the LVDS interface IC. Do not connect or disconnect the connector when the system power in on. Otherwise, the LVDS interface IC could be damaged.

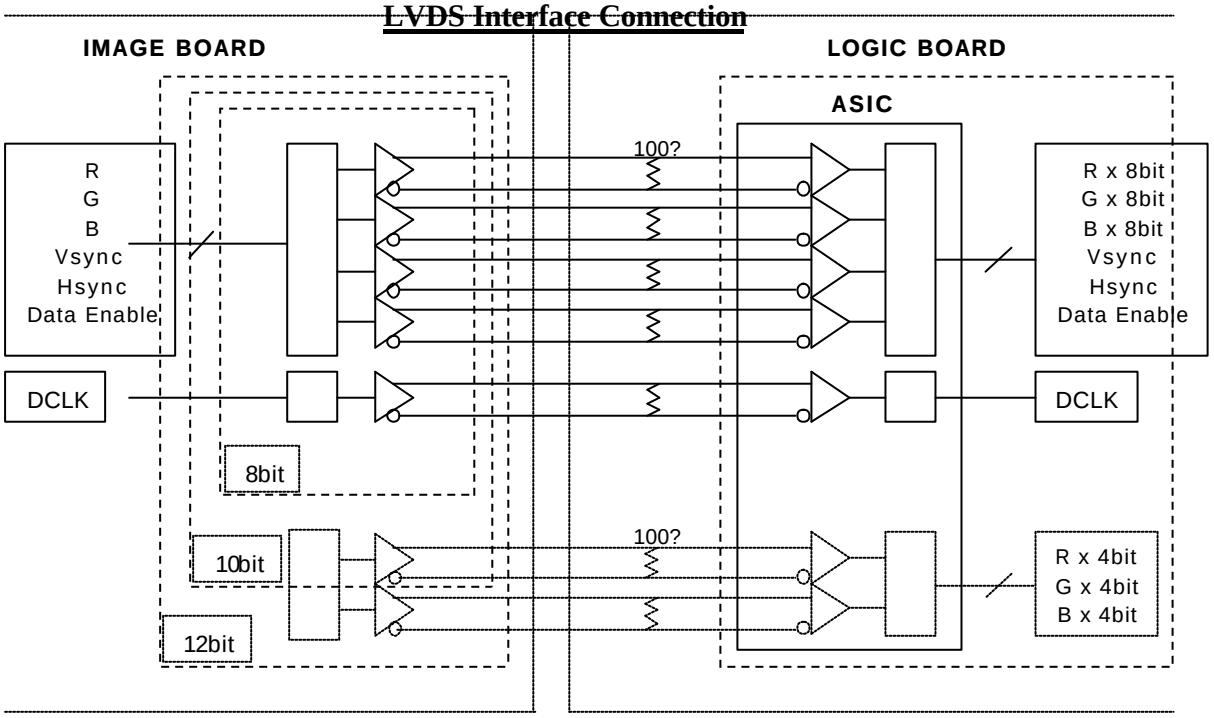


Figure-17. LVDS Interface Connection

10. 11 I2C Interface Conditions

10. 11. 1 Basic Specifications

This PDP Module has the I2C bus serial data communication function.
The customer may use this function to make settings for PDP Module characteristics of several items.

No	Parameter	Specifications
1	**Recommended** Transfer Rate	**50 kbps**
2	Device Status	Slave Receiver
3	Slave Address	CC(Write), CD(Read)

10. 11. 2 I2C–Ready Signal

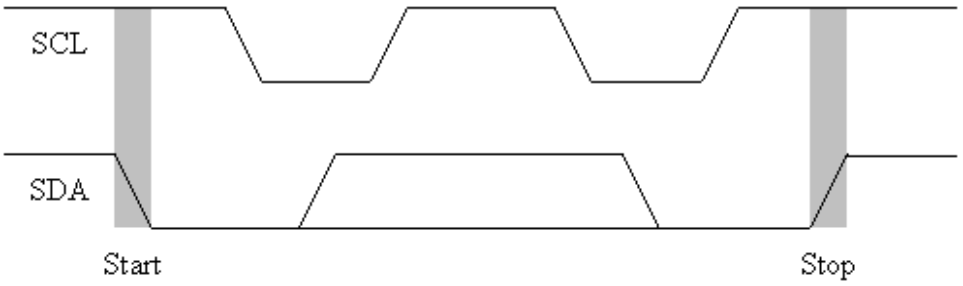
I2C control is available only when I2C-Ready signal is 'High' state.
I2C-Ready signal is assigned to pin number 22 of CN2020

10. 11. 3 Data Validity

Amount of data that is transferred is 1-Bit per 1 SCL cycle. Data is valid when SCL is high and recognized as to state of SDA.

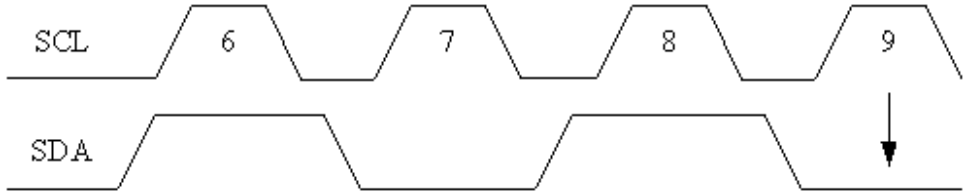
10. 11. 4 Start & Stop Condition

Start /Stop condition is generated by Master (=Image B'D). Before start condition or after stop condition, a SDA cannot be recognized as valid data.
Start condition ? SCL high & SDA transition from H to L
Stop condition ? SCL high & SDA transition from L to H


SCL
SDA
Start
Stop

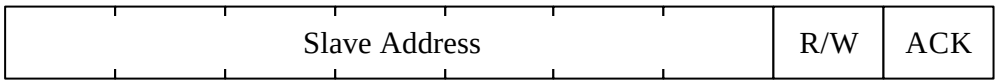
10. 11. 5. Acknowledge

When Master (=Image B'D) needs to stop reading data, the master should give NO ACK signal to salve by SDA. Slave (=PDP Module) gives ACK whenever 8-bit transfer is done.



10. 11. 6. 7-Bit Addressing for Device address(with example of CC or CD)

Master could choose slave by 7-bit slave address and decide what procedure is by R/W bit (H=Read procedure, L=Write procedure).

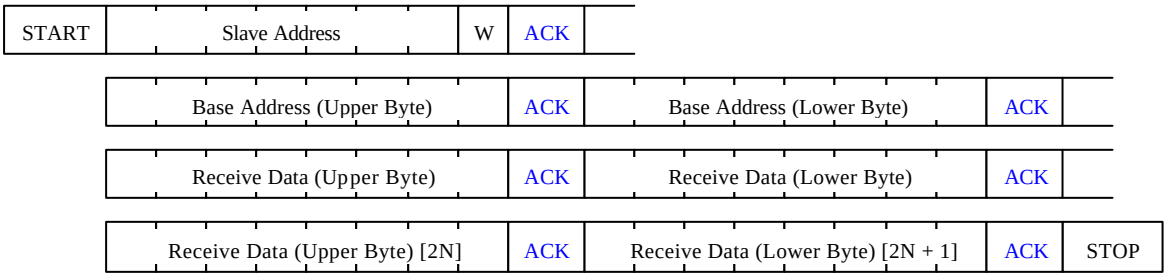


10. 11. 7. 16-Bit Mode

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

10. 11. 8 . Data Transfer Sequence (Write)

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').
Note 1: Black letters mean master (=Image B'D)'s bus occupation.
Note 2: Blue letters mean slave (=PDP Module)'s bus occupation.



10.11. 9. Data Transfer Sequence (Read)

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

Note 1: In advance, master should initialize writing sequence by giving base address and stop condition.

Note 2: After start condition and slave addressing, master could receive data from slave.

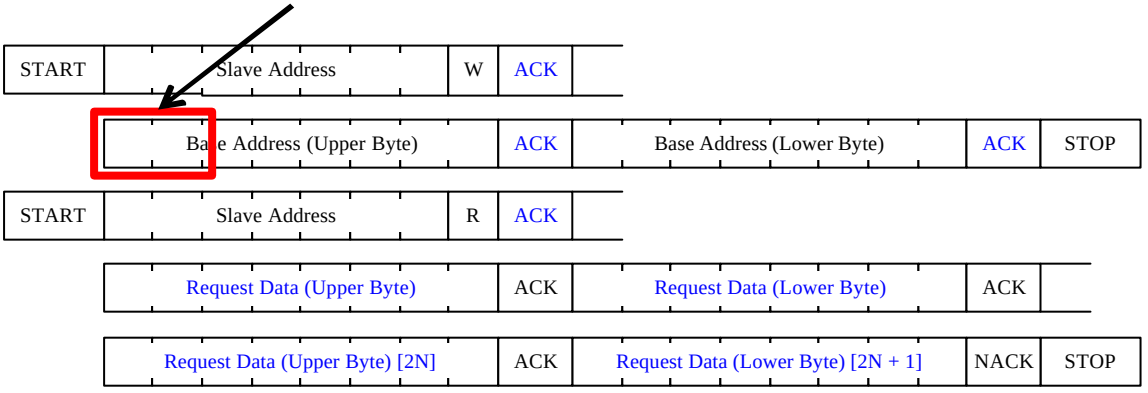
Note 3: Master should give acknowledge whenever 8-bit data is received.

Note 4: 'No acknowledge' could make master give stop condition on bus. Therefore, NACK is used for master to stop receiving data from slave.

Note 5: Black letters mean master (=Image B'D)'s bus occupation.

Note 6: Blue letters mean slave (=PDP Module)'s bus occupation.

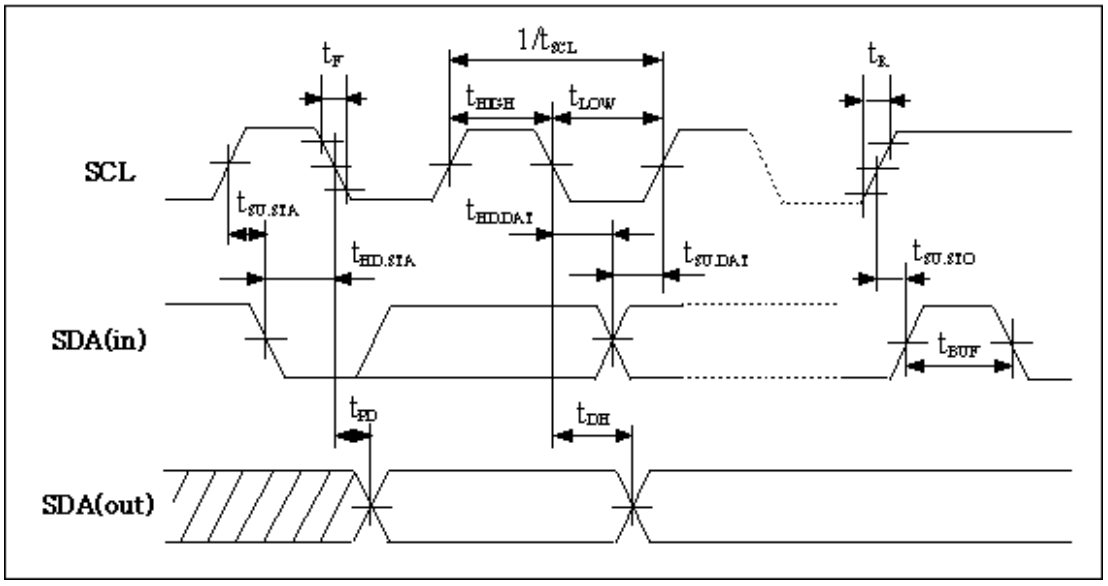
Note 7: **Option Bit = 11: both memory, 01: ROM (256K), 10: RAM (in ASIC)**



10. 11. 10. I2C Bus Timing Specifications

* Refer to the following data merely as sample data.

No	Item	Symbol	Standard			
			Min.	Typ.	Max.	Module
1	SCL Input Frequency	f_{SCL}	-	50	**75**	?
2	SCL Input "HIGH" Period	t_{HIGH}	0.3	-	-	?
3	SCL Input "Low" Period	t_{LOW}	0.5	-	-	?
4	Start Condition Set Up Time	$t_{SU.STA}$	0.3	-	-	?
5	Start Condition Hold Time	$t_{HD.STA}$	0.3	-	-	?
6	Data Input Set Up Time	$t_{SU.DAT}$	0.1	-	-	?
7	Data Input Hold Time	$t_{HD.DAT}$	0	-	-	?
8	Stop Condition Set Up Time	$t_{SU.STO}$	0.3	-	-	?
9	Data Output Delay Time	t_{PD}	0.1	-	-	?
10	Data Output Hold Time	t_{DH}	0.1	-	-	?
11	SDA Bus Free Time	t_{BUF}	0.5	-	-	?
12	SCL, SDA Input Rising Time	t_R	-	-	0.8	?
13	SCL, SDA Input Falling Time	t_F	-	-	0.3	?
14	SCL, SDA Line Capacitor	C_b	-	-	400	?



10. 12. Connector Specifications

Connector Name	Pin #	Signal Name
CN2020	3	TxOUT0-/RxIN0-
	4	TxOUT0+/RxIN0+
	7	TxOUT1-/RxIN1-
	8	TxOUT1+/RxIN1+
	9	TxOUT2-/RxIN1b-
	10	TxOUT2+/RxIN1b+
	11	TxOUT3-/RxIN2-
	12	TxOUT3+/RxIN2+
	15	TxCLKOUT0-/RxCLKIN-
	16	TxCLKOUT0+/RxCLKIN+
	17	TxCLKOUT1-/RxCLKINb-
	18	TxCLKOUT1+/RxCLKINb+
	19	TxOUT4-/RxIN3-
	20	TxOUT4+/RxIN3+
	22	I2C-READY
	23	TxOUT5-/RxIN0b-
	24	TxOUT5+/RxIN0b+
	25	IMG_EINT
	27	SCL (SEE notes 6)
	29	SDA (SEE notes 6)

NOTES:

1. CN2020 connector is located in Logic Board.
2. Pin to Pin pitch of connector CN2020 is 0.625? .
3. The length of mating cable to LA3 is recommended to be not longer than 25.0? .
4. Pin numbering order :
   right to left view from component side of Logic Board.
5. All the other pins are GND.
6. Reserved for factory use only. This pin should be disconnected in case of customer's use.
7. This pin is output pin. In case of fan failure, this signal becomes high.
8. IMG_EINT is operating LED signal of Logic Main.
   If not use, this pin should be N.C.

11.Address Map

11.1 Address Map

The I2C address map has three regions, i.e. NTSC / PAL common system area, NTSC-only system area and PAL-only system area..
The sub-address table shown below is for NTSC. The sub-address region for NTSC is 0000h~1FFFh, and that of PAL is 2000h~3FFFh
Basically address map for PAL is same as that of NTSC except the offset address. For example, 0080h for NTSC is correspondent to 2080h for PAL.

- I2C Slave Address ? Write: 66 (hex), Read: 66 (hex)

Sub Address	Data																Note
AF~0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0080			PS														R/W
0081					DL												R/W
0090														GTSEL			R/W
00D3									PUG								R/W
00D4									PLG								R/W
00E1									APCO								R/W

[Note]

1. Only sub-addresses shown in above table are allowable for access. An access to the any other address than shown in above sub-address table may lead to an abnormal system down or permanent damage.
2. 0000~007F : Area for NTSC/PAL common system registers .
   0080~1FFF : Area for NTSC-only system.
   2080~3FFF : Area for PAL-only system.

11.2 Details of Settings

Sub Address	Data Bit	Symbol	Item / Function	Setting [hex]			Note
				Range	Initial		
					NT	PAL	
0080(NT) 2080(PAL)	8~13	PS	**Pattern Select** ? Patterns below are valid when IE (Internal clk or External clk) is set to '1'. 00: Full Window (Black) 01~04: Full Window (White,Red,Green,Blue) 05 : 1 point Box(White, Windows size) 06~09: 9 Point Box (White,Red,Green,Blue) 0A : 1% Window , 0B: Color Bar 0C~0D: Gray Bar (Horizontal, Vertical) 0E: Half Gray, 0F:Cross Hatch, 10:Dot Array, 11:3% widow 12~13: 16step Gray Bar (Vertical, Horizontal) 14~15: Vertical Ramp Pattern (Stay, Scroll) 16~17: Horizontal Ramp Pattern (Stay, Scroll) 18 : Horizontal Ramp WRGB Pattern	00~17	01	01	*(a)
0081	8~15	DL	**Data Level** ? Patterns below are valid when **IE** (Internal clk or External clk) is set to '1'. 00~FFF : 0~ 4095 Gray Level.	000~FFF	FFF	FFF	*(a)
0090(NT) 2090(PAL)	0~2	GTSEL	**Gamma Table Selection** ? '0' : r = 2.0, '1' : r = 2.1, '2' : r = 2.2 '3' : r = 1.9, '4' : r = S curve.	0~4	00	00	*(b)
00D3(NT) 20D3(PAL)	0~7	PUG	**Power Upper Gain Control** ? Control the power upper level of PDP module.	00~FF	80	80	*(c)
00D4(NT) 20D4(PAL)	0~7	PLG	**Power Lower Gain Control** ? Control the power lower level of PDP module.	00~FF	80	80	*(c)
00E1(NT) 20D1(PAL)	0~7	APCO	**APC Offset Level** ? Adjusts peak luminance for customer's specifications.	00~C7	00	00	*(c)

*(a) Please access these address for test use only.
For ordinary operating conditions, values of these address should be set to initial values.

*(b) Customers can set these values considering their specifications.

*(c) APCO , PG is used for control the "Brightness and Power Mode" of PDP Module. For a detailed behavior and variable range, refer to the Chapter 6.7 Power Consumption**.**

12. Input Power Voltage Specifications

12.1 Electrical Characteristic Overview

Power Name	Voltage(V)	Max Load (A)	Regulation(%)	Ripple & Noise (mV)	Remarks
Vs	200	2.4	±1.5	1000	Sustain voltage
Va	65	3.5		500	Address voltage
Vscan	-200	0.1		500	Scan voltage
Ve	120	0.1		500	Bias voltage
Vset	190	0.2		500	Reset voltage
Vg	15	1.0	±5	100	Drive gate in FET
D5V	5.2	3.5		100	Drive TTL in X,Y driving, Logic
D3V3	3.4	5.0		100	Drive IC in Logic
12V	12.0	0.8		100	Image
5V	5.2	7.0		100	
29V	5.5	1.7		100	
S/B_5V	5.0V	1.0		50	Standby

***1. This means nominal voltage stability when current is changed from min to max.**

***2. The output voltages for Vs, Va, Vscan, Vset, Ve could be varied within variable range by feedback variable resistors.**

¦ Above voltage levels are norminal value. They are adjustable to drive Panel.

12.2 Detail Output Power Specification

12.2.1 DC outputs for Logic Board

Connector No.	Output Name	Nominal Voltage	Load Current(A)			Variable Range(V)	Remarks
			Min.	Nor.	Max.		
CN8010	D3V3	3.3	0.1	2.0	5.0	Fixed	
	D5V	5.2	0.1	2.0	3.5	Fixed	
	Vs_on	3.3V	-	-	-	-	Active High
CN8005	Va	65	0.1	1.0	3.5	65~75	

12.2.2 DC outputs for Driving Board(X,Y)

Connector No.	Output Name	Nominal Voltage	Load Current(A)			Variable Range(V)	Remarks
			Min.	Nor.	Max.		
CN8002 CN8003	D5V	5.2	0.2	-	1.0	Fixed	
CN8002 CN8003	Vg	15	0.5	0.5	1.0	Fixed	
CN8002	Ve	120	0.01	0.07	0.1	110~130	<Vs
CN8003	Vset	190	0.01	0.05	0.2	180~200	<Vs
CN8003	Vscan	-200	0.01	0.05	0.1	-190~ -210	
CN8002 CN8003	Vs	200	0.1	2.0	2.5	190~210	

12.2.3 DC outputs for Image board

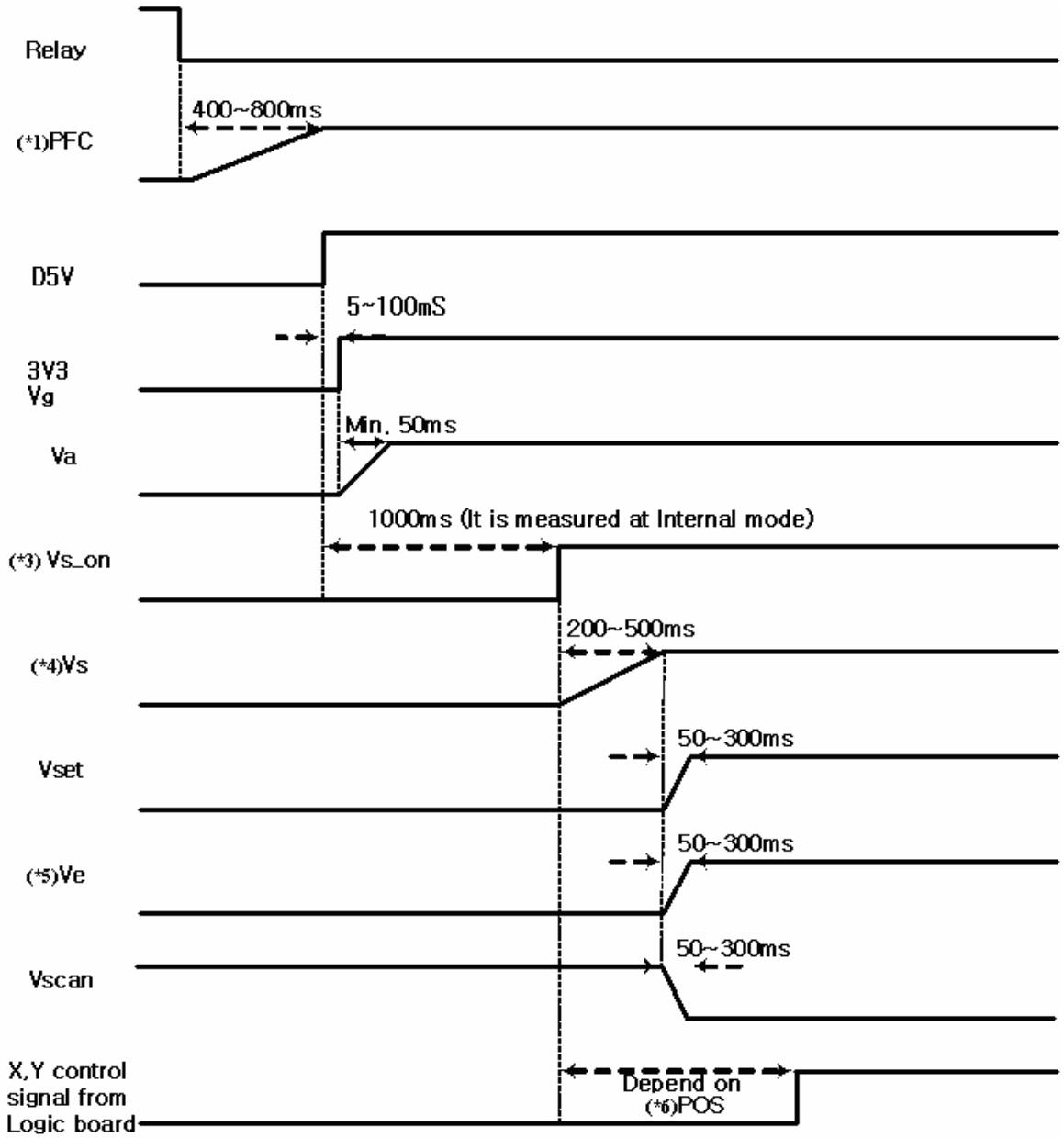
Connector No.	Output Name	Nominal Voltage	Load Current(A)			Variable Range(V)	Remarks
			Min.	Nor.	Max.		
CN8007	S/B 5V	5.0	0.1		1.0	Fixed	Standby
CN8004 CN8007	D5V	5.2	0.1		7.0	Fixed	
CN8007	12V	12	0.1		0.8	Fixed	
CN8007	29V	29	0.1		1.7	Fixed	

12.2.4 Out Dimension for reference

Length(mm)	Width(mm)	Height(mm)	Remark
445mm	245mm	Max. 40mm	From PCB top

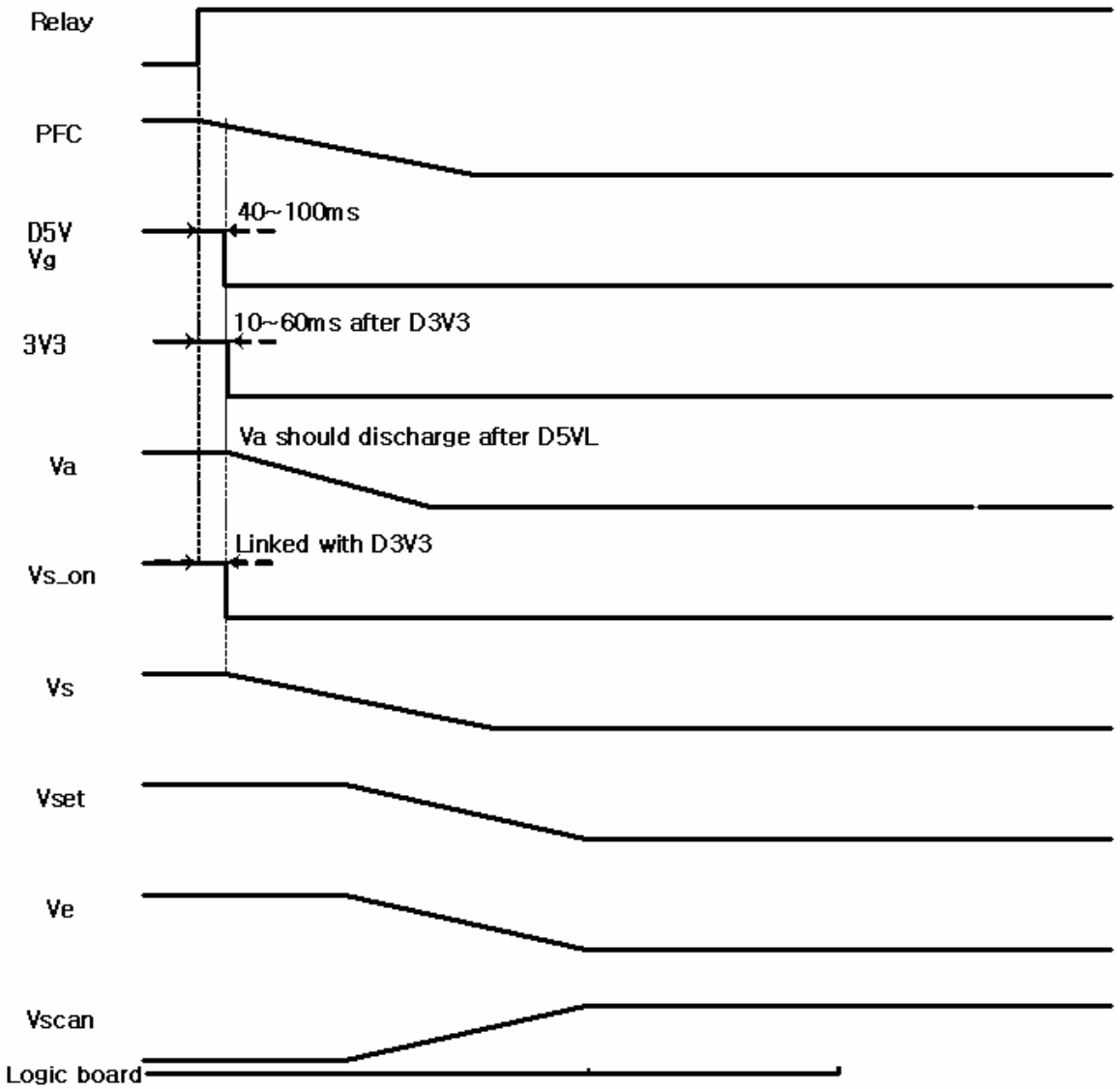
12.3 Power Applying Sequence

? **Relay_on Sequence**



***1. Reference value**
***2. D3V3 needs to start with 5~50ms rising time . And at least 500mA is needed for rising time.**
***3. Vs_on signal is output from Logic board to PSU.**
***4. Vs should be enable with Vs_on signal(Active High) from Logic.**
***5. Vs should be always higher than Ve while D3V3 is alive.**

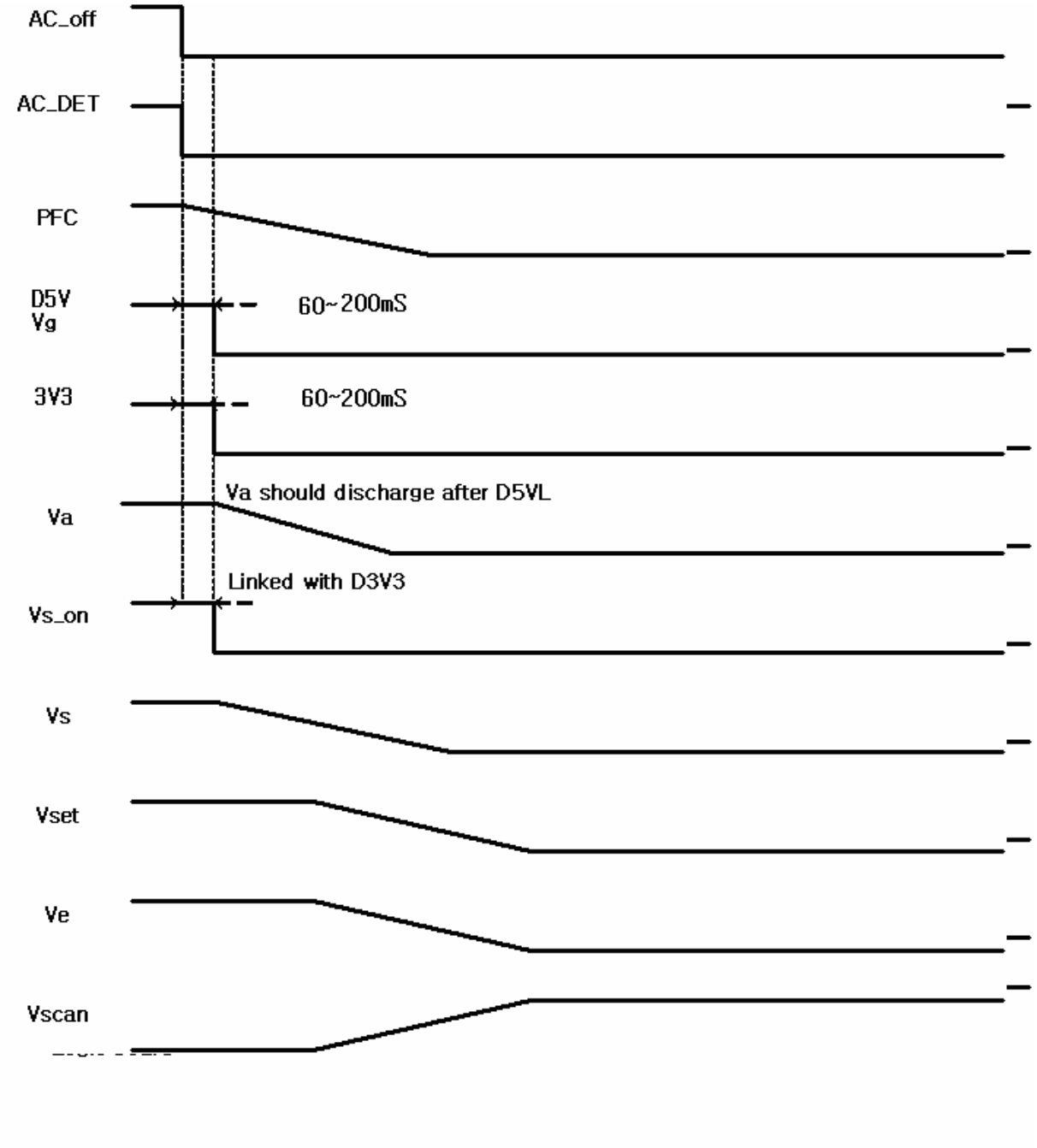
? **Relay_off Sequence**



***1. D3V3 discharge should be faster than other voltages.**

¦ **Either spontaneous discharge or active discharge is available for PFC, Vs, Va, Vset, Vscan, Ve as long as D3V3 has discharged before other voltages.**

? AC_off Sequence



***1. D3V3 discharge should be faster than other voltages.**
D3V3 should discharge before Vg voltage level is 11V and Vs voltage level is lower than Ve.
¦ Either spontaneous discharge or active discharge is available for PFC, Vs, Va, Vset, Vscan, Ve. as long as D3V3 has been discharged before other voltages.

12.4 Pin assignment of connectors for Power Supply

Location No	CN8001	CN8002	CN8003	CN8004	CN8005
Function	AC Input	X-Main	Y-Main	Image	Logic Buffer
Pin Num.	3pin	9pin	10pin	12pin	5pin
Type	JST B2P3-VH	Molex 35313-0910	Molex 35313-1010	JST B12B-PHDSS	Molex 35313-0510
Pin No.	Pin Name	Pin Name	Pin Name	Pin Name	Pin Name
1	Live	5V	Vs	5V	Va
2	N.C	Vg	Vs	5V	N.C
3	Netural	GND	GND	5V	D5V
4		GND	GND	5V	N.C
5		Ve	Vset	5V	GND
6		GND	GND	5V	
7		GND	Vscan	GND	
8		Vs	GND	GND	
9		Vs	Vg	GND	
10			D5V	GND	
11				GND	
12				GND	

Location No	CN8006	CN8007		CN8010
Function	Image	Image		Logic Main
Pin Num.	2pin	20pin		10pin
Type	Molex 35312-02	Yeon Ho YDW200-20(BLACK)		Molex 35312-10
Pin No.	Pin Name	Pin Name		Pin Name
1	29VAMP	NC	GND	D3.3V
2	GND	NC	GND	D3.3V
3		NC	5V	GND
4		THEM-D	5V	GND
5		12V	5V	5V
6		*1_ PS-ON	5V	GND
7		GND	GND	*3_Relay On
8		GND	GND	NC
9		GND	*2_5V-S/B	*4_Vs_ON
10		GND	5V-S/B	5V

*1. This is a signal(Active low) from I/B to PSU. (High : 5V, Low : 0V)

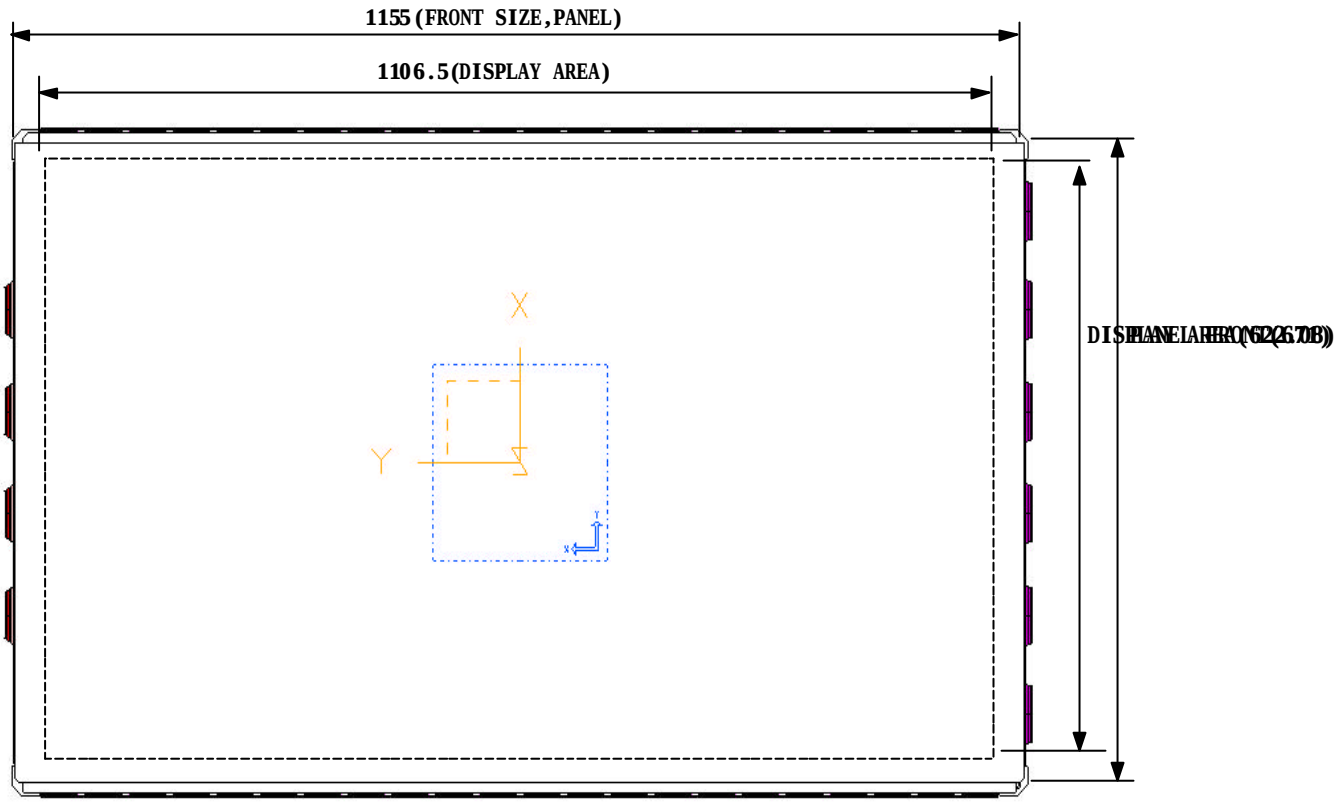
*2. This is a standby voltage which is used for I/B. (On : 5V, Off : 0V)

*3. This is a signal(Active High) from Logic main to PSU. (High : 3.3V, Low : 0V)
PSU relay on/off function is controlled by Logic micom.

*4. This is a signal(Active High) from Logic main to PSU. (High : 2.8V, Low : 0V)

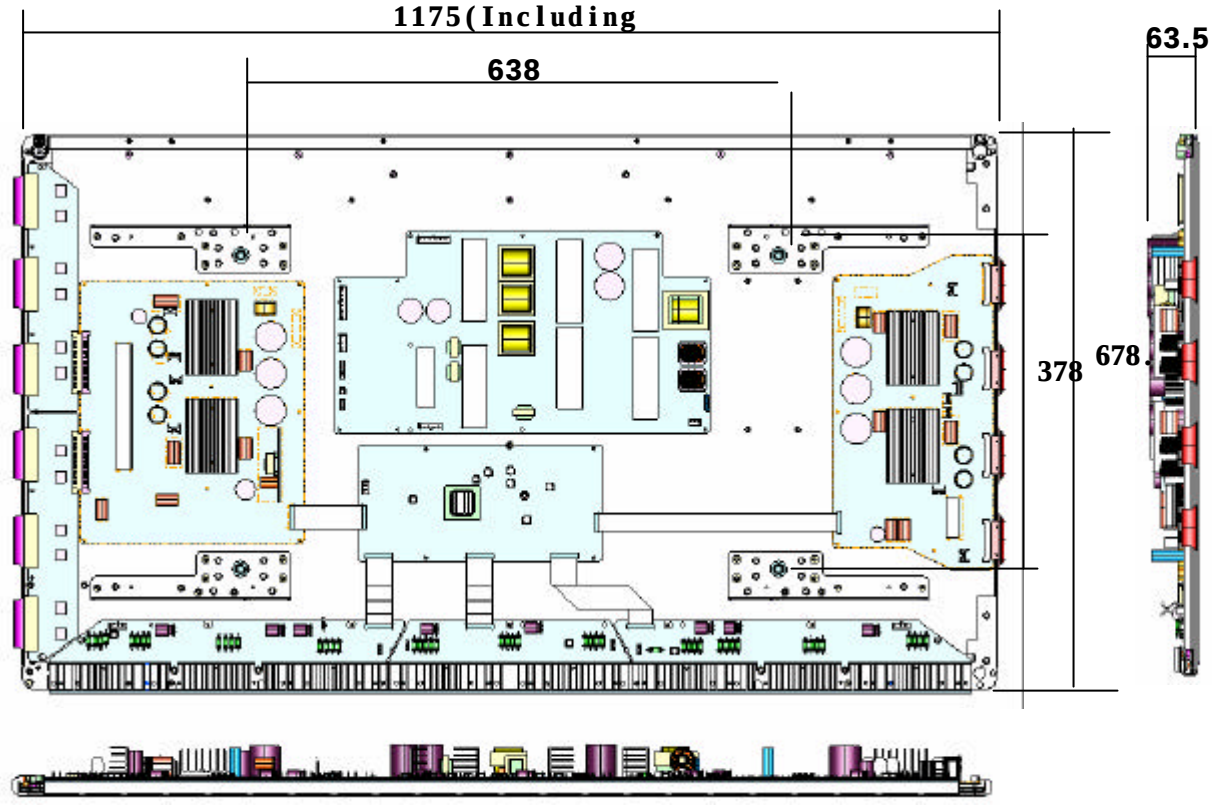
13. Mechanical Dimension Drawing

13.1. Front Side



Appendix A1

13.2. Rear Side

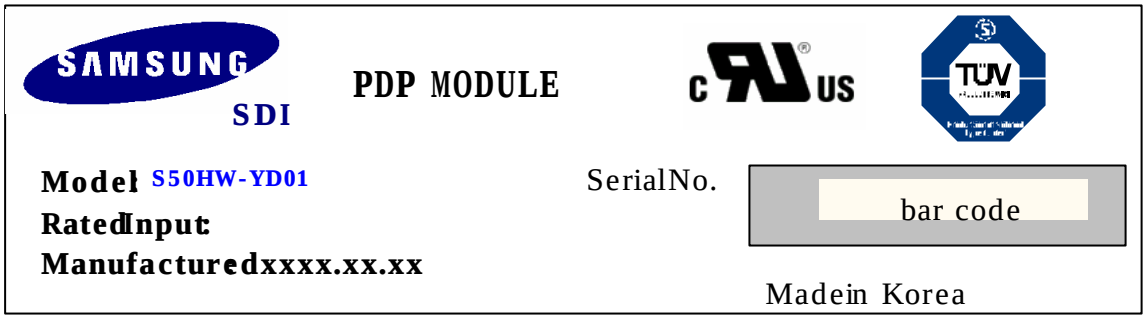


Appendix A2

14. Label

14.1 Label Type

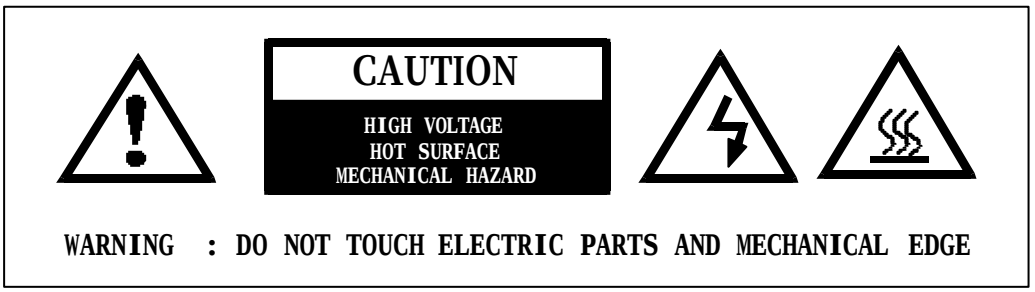
(1) Label for the PDP Module



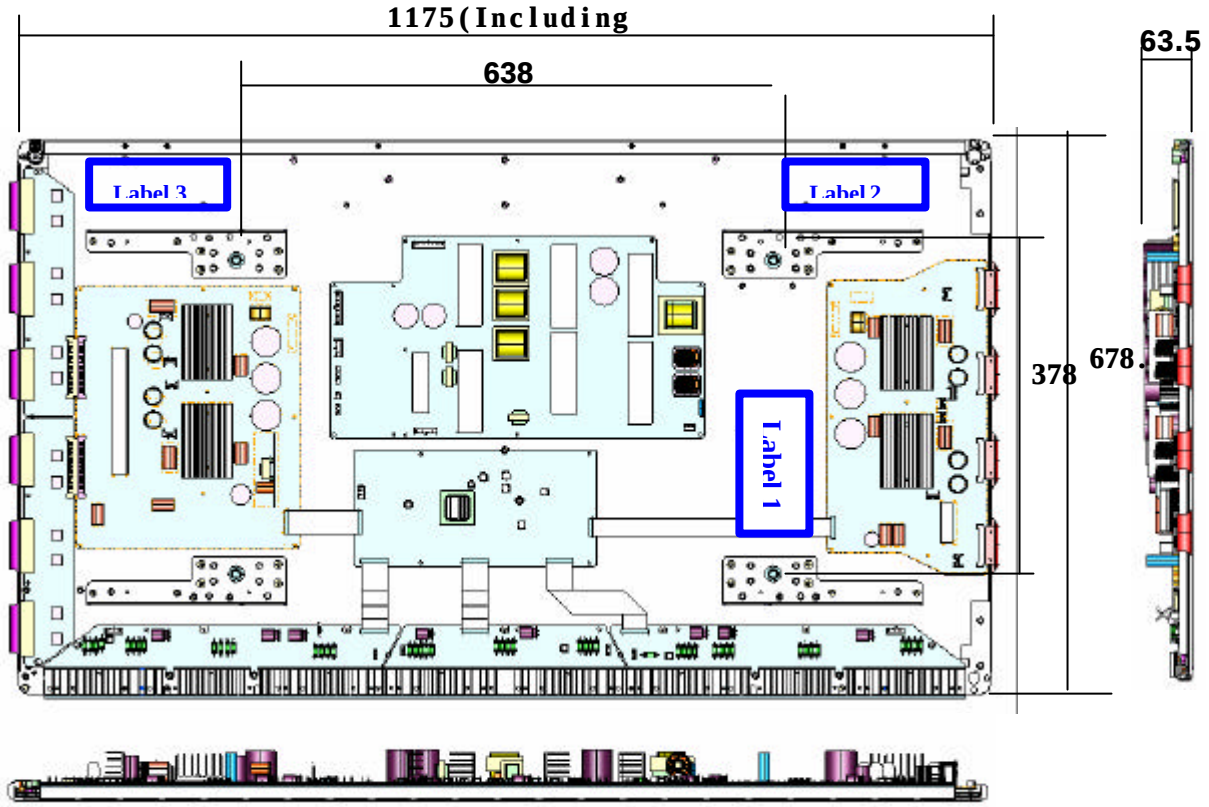
(2) Label for power specification

? NTSC			?√ NTSC/PAL		
Va	Vsc	Vs	Ve	Vset	
VSB	D5V	D15V	VAUDIO	VFAN	

(3) Caution Label



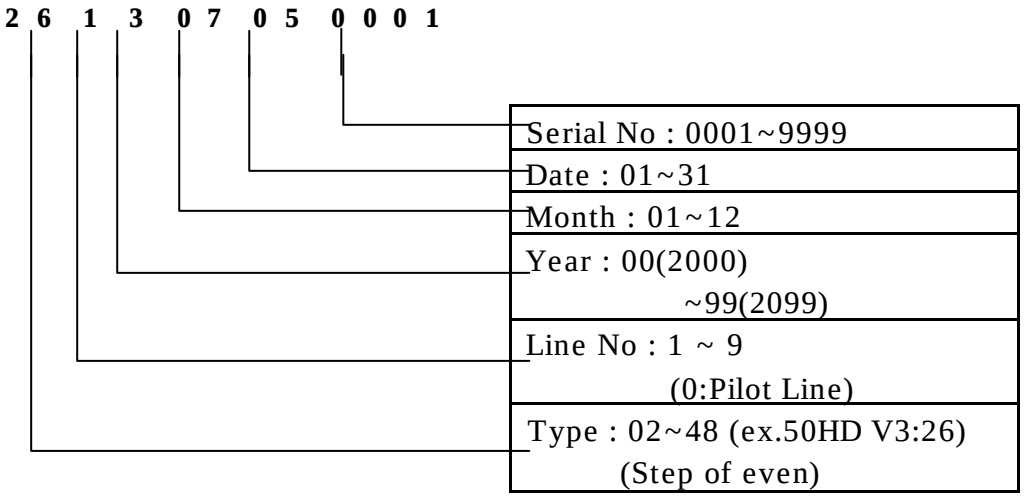
14.2 Label location (TBD, To be updated)



? Notes ?

1. Label-1 is a label for the PDP Module.
2. Label-2 is a label for the power specification.
3. Label-3 is a lable for the Caution Label

14.3 Serial No.



15. Packing

15.1 Packing Dimension and Parts List

- Number of Module in 1 package: 6Modules
- Packing dimensions (W*L*H): 1465*760*1106 (mm) (Including Pallet :136mm)
- Weight: About 209 ± 5 (Kg)

-

No.	Parts	Specification	Q'ty	Remarks
1	Bag PE	W1229,L723,T0.5	1,200	(Unit: Module 1200 pcs)
2	Silicagel(DRY-PAK)	100g	2,400	
3	Packing-Module	HIPS,HB,BLK	1200	
4	Screw,Machine	PH,+,M8,L25	4,800	
5	Pallet	L1465,W728,H136	200	
6	Packing-Cover-Top	DW 1745× 1007× 10T	200	
7	Packing-Cover-Bot	DW 1745× 1007× 10T	200	
8	Cushion-Set	50HD,EPP,C=0.022	200	
9	Band,PE	T1,W18mm	800M	
10	Guide,Pack	L1465,D50,T5	400	

15.2 Packing Assembly Drawing

(To be included)

16. RELIABLITY

16.1 MTBF Value

Mean Time Between Failure is dependent on the overall PDP Module design.

MTBF : 20,000hours (environmental temperature : 25?)

? Condition : 25? , Used moving Picture Signal

16.2 Expected Service Life

#1. Definition

The expected service life is defined by the following two categories.
And the life time is defined by either (1) or (2), whichever occurs first.

(1) The white color Luminance level becomes half (50%) of its initial value, which is determined by the phosphor characteristics.

(2) The number of display cell defects increases to double the specification value, which is depending on the discharge characteristics.

#2. Test condition and life time

The expected service life time varies depending on the display conditions set forth below.

(1) Full screen white color display

Life time : 30,000 hours

* Test condition : 8Hr/Day

17. WARNING / CAUTION / NOTICE

TO PREVENT POSSIBLE DANGER, DAMAGE, AND BODILY HARM, PLEASE CONSIDER AND OBSERVE ALL WARNINGS AND CAUTIONS CONTAINED IN THIS PARAGRAPH.

17.1 Warning

If you do not consider the following warnings, it could result in death or serious injury

(1) The S50HW-YD01 Module is controlled by high voltage about 350V. If you need to handle the Module during operation or just after power-off, you must take proper precautions against electric shock and must not touch the drive circuit portion and metallic part of S50HW-YD01 Module within 5 minutes.
The capacitors in the drive circuit portion remain temporarily charged even after the power is turned off. After turning off the power, you must be sure to wait at least one minute before touching the Module. If the remain voltage is strong enough, it could result in electric shock.

(2) Do not use any other power supply voltage other than the voltage specified in this product specifications. If you use power voltage deviated from the specifications, it could result in product failure.

(3) Do not operate or install under the deviated surroundings from the environmental specification set for the below; in moisture, rain or near water-for example, bath tub, laundry tub, kitchen sink; in a wet basement; or near a swimming pool; and also near fire or heater - for example, near or over radiator or heat resistor; or where it is exposed to direct sunlight; or somewhere like that. If you use the S50HW-YD01 Module in places mentioned above, it could result in electric shock, fire hazard or product failure.

(4) If any foreign objects (e.g. water, liquid and metallic chip or dust) entered the S50HW-YD01 Module, the power supply voltage to the S50HW-YD01 Module must be turned off immediately. Also, never push objects of any kind into the S50HW-YD01 Module as they may touch dangerous voltage point or make short circuits that could result in fire hazard or electric shock.

(5) If smoke, offensive smell or unusual noise should come from the S50HW-XD03 Module, the power supply voltage to the S50HW-YD01 Module must be turned off immediately.
Also, when the S50HW-YD01 screen fails to display any picture after the power-on or during operation, the power supply must be turned off immediately. Do not continue to operate the S50HW-YD01 Module under these conditions.

(6) Do not disconnect or connect the S50HW-YD01 Module's connector while the power supply is on, or immediately after power off. Because the S50HW-YD01 Module is operated by high voltage, and the capacitors in drive circuit remain temporarily charged even after the power is

turned off. If you need to disconnect or reconnect it, you have to wait at least one minute after power off.

(7) Do not disconnect or connect the power connector by a wet hand. The voltage of the product may be strong enough to cause an electric shock.

(8) Do not damage the power cable of the S50HW-YD01 Module, also do not modify it.

(9) When the power cable or connector is damaged or frayed, do not use it.

(10) When the power connector is covered with dust, please wipe it out with a dry cloth before the power on.

17.2 Caution

If you do not consider the following cautions, it may result in personal injury or damage facilities.

(1) Do not set the S50HW-YD01 Module on an unstable place, vibrating place and inclined place. The S50HW-YD01 Module may fall or collapse, and it may cause serious injury to a person, and serious damage to the product.

(2) If you need to remove the S50HW-YD01 Module to another place, you must turn off the power supply and detach the interface cable and power cable from the S50HW-YD01 Module beforehand, and watch your steps not to step on the cables during the operation. If the cables are damaged during the transport, it may result in fire hazard or electric shock. Also if the S50HW-YD01 Module is dropped or fallen, it may cause a serious injury to a person.

(3) When you draw or insert the S50HW-YD01's cable, you must turn off the power supply and do it (with) holding the connector. If you forcibly draw the cable, the electric wire in the cable can be exposed or broken. It may result in fire hazard or electric shock.

(4) When you carry the S50HW-YD01 Module, it should be done with at least two workers in order to avoid any unexpected accidents.

(5) The S50HW-YD01 Module has a glass-plate. If the S50HW-YD01 Module is inflicted with excessive stress - for example; shock, vibration, bending or heat-shock, the glass plate could be broken. It may result in a personal injury. Also, do not press or strike the glass surface.

(6) If the glass panel was broken, do not touch it with bare hand. It may result in a cut injury.

(7) Do not place any object on the glass panel. It may be the cause of the scratch or break of the glass panel.

(8) Do not place any object on the S50HW-YD01 Module. It may result in a personal injury due to fall or drop.

17.3 Notice

When you apply the S50HW-YD01 Module to your system or handle it, you must make sure to follow the notices set forth below.

? Notice to your system design

(1) The S50HW-YD01 Module radiates the infrared rays of between 800 and 1000? . It may bring an error in operating the IR-remote controller or another electric system. Please consider (to) providing the IR absorb filter in your system, and evaluating it.

(2) The S50HW-YD01 Module has a high-voltage switching circuit and a high-speed clock circuit. Therefore, you have to apply and evaluate the EMC consideration of your system.

(3) The S50HW-YD01 Module has a glass plate. In your mechanical design, please (consider to) avoid any excessive shock and stress to the glass surface. Also be careful not to demage the tip-tube at the corner of glass plate. If the glass plate and tip-tube are damaged, the S50HW-YD01 Module may fail.

(4) In your system, for your safety, please have the remaining voltage of the S50HW-YD01 Module leaked immediately after power-off.

(5) As the S50HW-XD04Module generates heat during operation, please make sure the well-radiation and well-ventilation are provided for your system design. The S50HW-YD01 Module may be defected by the usage out of the specified ambient temperature.

(6) The ventilation design in your system should have a back-cover that is able to prevent moisture and dust from getting into the inside of the electric circuit, because the S50HW-YD01 Module has high-density electric parts with high-voltage. If the driver circuit has condensation or dusts, it may cause a short circuit or dielectric breakdown.

(7) If the S50HW-YD01 Module displays a fixed pattern on the screen for are extended period of time, it could make the differences in Luminance and chromaticity between fixed pattern area and other areas. It is because the Luminance of the fixed pattern area becomes lower than the other areas due to the degradation of the phosphor, but this phenomenon is not a failure.
On the other hand, when the display pattern is changed, the illuminated areas may maintain their Luminance temporarily (for few minutes). This phenomenon is a characteristic from color S50HW-YD01 itself due to the activation of the discharge surface in the S50HW-YD01 panel, which is normal. If you have an intention of displaying the fixed pattern, the screen-saver technique should be applied to your systems in order to minimize the image retention.

(8) The S50HW-YD01 Module is not intended for the equipments that require extremely high reliability such as aerospace equipments, nuclear control systems or medical equipments for life support.

(9) Based on the requirements of the safety standard (UL, EN etc.), be sure to add the filter that come up to the impact test to the glass pate.

? Notice to the operation and handling of the S50HW-YD01 ***Module***.

(1) To prevent defect or failure, please check the cable connections and power-supply condition before power-on.

(2) The S50HW-YD01 Module is controlled by high voltage. Not only during operation but also immediately after power-off, do not disconnect or reconnect the S50HW-YD01 Module's connector because it may result in failure. If you need to disconnect or reconnect, you have to wait at least one minute after power-off.

(3) The S50HW-YD01 Module is equipped with various protection circuits that automatically stop the Module operation, if an interface signal or the power voltage becomes abnormal during operation. If the S50HW-YD01 Module stops suddenly during operation, please check the conditions of input signal or power source before restarting.

(4) For the protection of the circuit, if an abnormal situation is occurred, the high output voltage will be shut down by (watching) the internal input voltage (Vs/ Va/ Vcc). In this case, the Module power resetting is necessary to recover.
There are also fuses in the Vs and Va power supply system to prevent smoking and firing by the excessive current. The protecting function of the address driver of keeping a supervisory device for the internal current is provided in the Va power supply system. Therefore, the number of sub-frames decreases to a proper value when the Ia current exceeds a constant value occasionally.

(5) If an abnormal situation such as disconnecting of the input connector occurs, this Module will be on stand-by, which the supply of high output voltage is stopped even if an external power is being supplied. If a normal signal is inputted after this, normal operation state, operations can be restarted again by re-inputting a normal signal. However, it is necessary to rest the Module power when tVH and/or tHV are less than the minimum value provided in the specification

(6) To ensure reliable operation of the S50HW-YD01 Module and to protect it from overheating, do not wrap or cover it with a cloth or like a sheet during power-on period. Also, do not place the S50HW-YD01 Module in a confined space or any other places of poor ventilation.

(7) If you continue to watch the naked S50HW-YD01 screen(without filter glass) for a long time, your eyes could be fatigued. We recommend you rest your eyes occasionally.

(8) The S50HW-YD01 screen is controlled with the display-data signals and synchronized signals. If noise interferes with those signals, the S50HW-YD01 screen could become unstable and, in some case, would cause a failure. Do not place any equipment that generates excessive EMI/RFI noise near the interface cable of the S50HW-YD01 Module, and keep the cables as short as possible.

(9) Be careful not to break the glass panel when you handle the S50HW-YD01 Module. Also, when handling the S50HW-YD01 Module, you must wear gloves or other hand protection to prevent injuries that can occur in case when the glass panel is broken.

(10) The glass panel section and drive circuit section of the S50HW-YD01 Module are closely connected and they function as a pair. If the Module is arbitrarily recombined, restructured, or disassembled, SDI will not be responsible for the function, quality, or operational integrity of the modified Module. Do not recombine, restructure, or disassemble it.
(only, the Module for A/S is allowed to be recombined, restructured, or disassembled.)

(11) To avoid a possible electric shock, you must make sure that the power supply voltage of S50HW-YD01 Module is turned off before cleaning. To clean the S50HW-YD01's glass panel, apply water or a natural detergent to a piece of soft cloth or gauze, and wring the cloth tightly before wiping the screen. Make sure that no water comes in contact with the connecting terminals on the side of the glass panel. Do not use chemical solvents, such as paint thinner or benzene, to clean the glass panel.

(12) The drive circuit section of S50HW-YD01 Module uses C-MOS integrated circuits that must be protected from static electricity. Therefore when transporting or delivering the Module, be sure to put the Module in an antistatic bag. When handling the S50HW-YD01 Module, take adequate grounding precautions to prevent static electricity.

(13) When delivering or transporting the S50HW-YD01 Module, you must take special precautions because excessive vibration or shock should not be applied to it. If the Module is dropped, or (if) excessive vibration/shock is applied, the glass panel of the S50HW-YD01 Module may be broken and the drive circuit may be damaged. The packing for delivering or transporting should be made with strict instructions.

(14) When storing the S50HW-YD01 Module, you must select an environmentally controlled place. Avoid any environment in which the temperature or humidity exceeds the specification values. If you are storing it for a long period of time, We recommend that you place the Module together with a dehumidifying agent, such as silica gel, in a moisture-proof bag and keep it in an environmentally controlled place.

(15) The S50HW-YD01 Module is composed of various kinds of materials such as glass plate, metals and plastics. A qualified service technician is required for the disposal of the S50HW-YD01 Module.

? Notice of the S50HW-YD01 Module performance

The S50HW-YD01 Module is the newest display device utilizing the gas discharge technology and digital signal processing technology, and its performances are mostly similar to those of CRT. However, some display performances of the S50AX -****Module are different from the CRT's. Please consider the following notices when you watch the S50HW-YD01 screen.

(1) There is (a) slight Neon luminance shown outside of the effective display area on the glass panel.

Conceal this part so that it may not be seen on the display surface.

(2) Depending on the type and time of usage, there may be a slight change in the Luminance and color. There may be an increase of both X-value and Y-value by 0.05 at the maximum in chromaticity. In this case, adjust it using the external data signal.

(3) Because the S50HW-YD01 Module uses phosphor to emit a light, the phosphor, like a CRT, will be deteriorated in proportion to the display signal and Luminance settings. If the same pattern is displayed continuously (fixed display) for an extended period of time, the Luminance of that area will be decreased over non-lit areas due to the fact that the discharge surface will be more activated comparing to the other areas.

(4) When the Vsync signal timing becomes shorter right after the changing of Vsync frequency (e.g. from 50? to 60H / from 60? to 70?) depending on the Multi-Vsync function, an initial Vsync signal of the changed frequency will be disregarded and the S50HW-YD01 screen will be interrupted for 1 frame period in maximum.

(5) Because the S50HW-YD01 Module is a digital processing display device, this Module is equipped with the Error diffusion technology and a Duplicated Sub-Frame method to display the grayscale and false contour improvement. However, you may sometimes find a color false contour, especially in human facial contour, in moving picture due to the difference of display performance comparing to the TV-tube.

(6) If the S50HW-YD01 Module displays some video test patterns that are mostly used in a laboratory or inspection process of the manufacturing facilities, you may find the following subjects. But these subjects sould not be recognized in the failure or defects because the display performance of the S50HW-YD01 Module is equipped with Error diffusion technology and Duplicated Sub-Frame method(for PAL) based on digital processing technique.

<a> Linearity in the grayscale test pattern

If the S50AX -****Module displays the grayscale test pattern (e.g. white color Luminance is gradually changed horizontally or vertically) in a screen, you may find the disparity of Luminance at adjacent grayscale patterns. This behavior is caused by duplicated sub-frame condition(for PAL), display load correction and electrode dependency.

<b> Color contouring and dithering at the stationary picture

If the stationary picture such as a human face or the like is shown in the S50HW-YD01 screen, you may feel some unstable noise at the contour area. This behavior is called the color contouring or dithering, and is caused by the error diffusion condition, display load correction and electroad dependency.

(7) If the S50HW-YD01 Module is operated under inadequate conditions or harsh environment, the screen may become unstable or noisy. This instability is mostly related to ambient temperature, air pressure, input signal instability (include signal noise), input power voltage and strong magnetic field such as MRI/NMR application or superconducting magnet application. Please do not apply the

S50HW-YD01 Module to inadequate conditions or harsh environment mentioned above.

Disclaimer

This Specification stipulates the final and comprehensive requirements for the respective products hereof. Beyond this Specification, it is the responsiblity of the customer to explicitly disclose any additional requirements, information or reservations regarding these requirements to Samsung SDI prior to implementation, where any and all disclosures of the customer shall be with an authorized representative of Samsung SDI in writing. Samsung SDI shall not be responsible for safety, performance, functionality or compatability of the system with which the Samsung SDI-supplied components are intergrated unless such features have been expressly communicated and described in the Specification. SAMSUNG SDI MAKES NO GUARANTY OR WARRANTY, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, TO ANY PARTY. Moreover, any party should do their own due diligence regarding these requirements prior to implementation.